

COMPAL CONFIDENTIAL

MODEL NAME : QALAI
PCB NO : LA-7762A (DAZ0LI00100)
BOM P/N : 4519EJ31L01,4519EJ31L02,4519EJ31L03,4519EJ31L04.
GPIO P/N: E4 VC GPIO map rev 1.1

Dalmore 15 DSC

Ivy Bridge + Panther POINT

2012-03-13

REV : 1.0 (A00)

@ : Nopop Component

CONN@ : Connector Component

MB Type	BOM P/N	
TPM	4319EJ31L01(R3) 4319EJ31L03(R1)	1@ 3@ PS8171@
DTP	4319EJ31L02(R3) 4319EJ31L04(R1)	2@ 3@ PS8171@

MB PCB	
Part Number	Description
DA80000P600	PCB 0LI LA-7762P REV0 M/B DSC

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Title

Cover Sheet

Size

Document Number

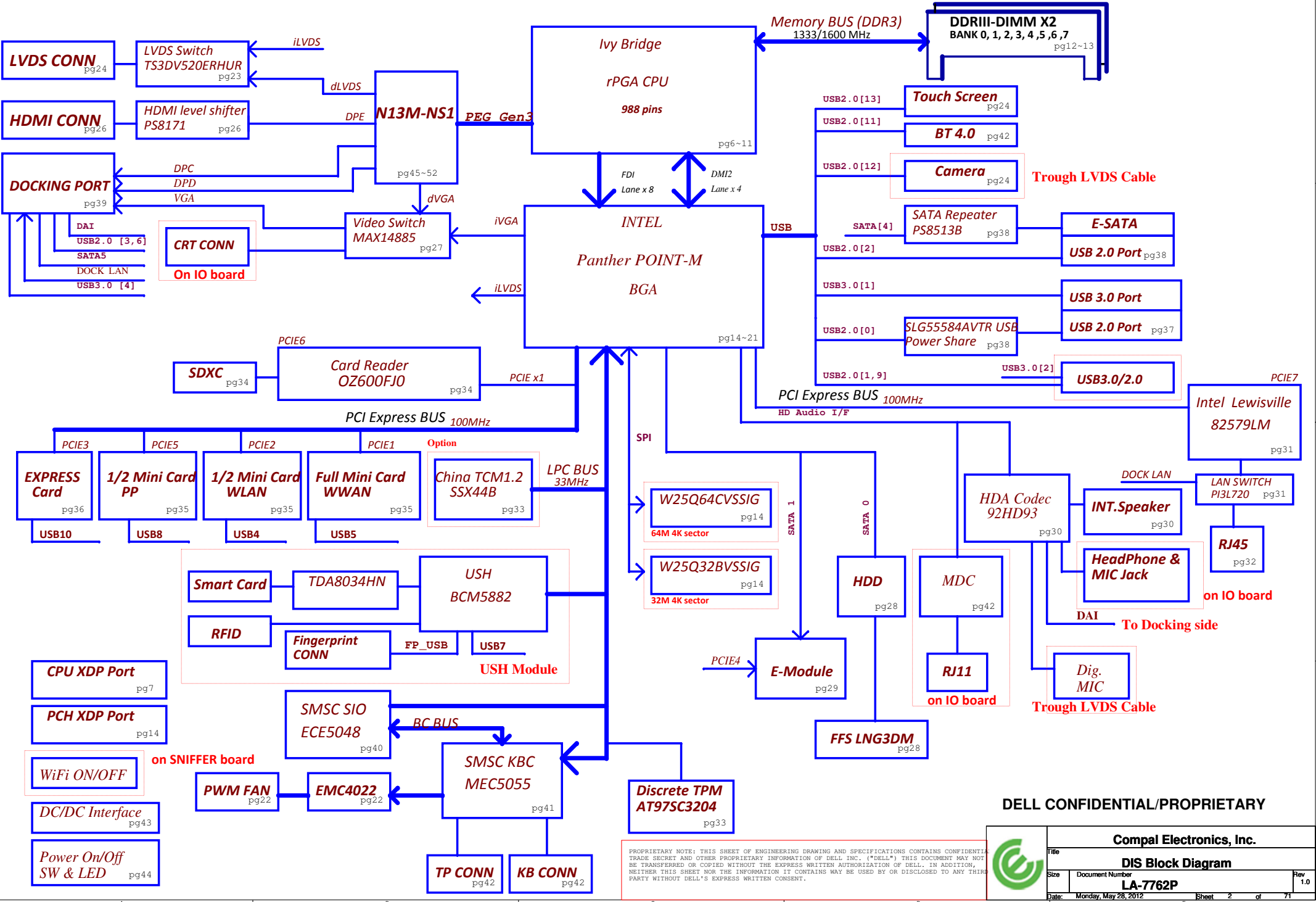
LA-7762P

Rev

1.0

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DIS Block Diagram			
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POWER STATES

Signal State	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

USB 3.0 PORT#	Connetion
1	JUSB1 (Right side)
2	JUSB2 (Left side)
3	NA
4	DOCKING

PCH	USB PORT#	DESTINATION
	0	JUSB1 (Right side)
	1	JUSB2 (Left side)
	2	JESA1 (Right side ESATA)
	3	DOCKING
	4	WLAN/WIMAX
	5	WWAN/UWB
	6	DOCKING
	7	USH->BIO
	8	JMINI3(Flash)
	9	JUSB (Left side)
	10	Express card
	11	Bluetooth
	12	Camera
	13	LCD Touch

USH	0	BIO
	1	NA

PM TABLE

power plane State	+PWR_SRC +PWR_SRC_S +5V_ALW +3.3V_ALW +3.3V_RTC_LDO	+3.3V_SUS +1.5V_MEM +3.3V_ALW_PCH +5V_ALW_PCH	+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +0.75V_DDR_VTT +VCC_CORE +1.05V_RUN_VTT +1.05V_RUN +GPU_CORE	+3.3V_M +1.05V_M (M-OFF)	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC don't exist	OFF	OFF	OFF	OFF	OFF

SATA	DESTINATION
SATA 0	HDD
SATA 1	ODD/ E3 Module Bay
SATA 2	NA
SATA 3	NA
SATA 4	ESATA
SATA 5	Dock

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	Express card
Lane 4	E3 Module Bay (USB3)
Lane 5	1/2 MINI CARD-3 PCIE
Lane 6	Card Reader
Lane 7	10/100/1G LOM
Lane 8	None

Layer No.	Name	Er	Material	Thickness (Material SPEC.) Unit : mil	Thickness (Actuality) Unit : mil
			SolderMask	IT-158	0.50
			Add Plating		1.30
1	Top		Copper foil	0.5oz	0.65
		3.7	Prepreg	1080	2.40
2	GND1		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
3	Sig 1		Copper foil	1.0 oz	1.35
		4.3	Prepreg	1506+7628H	13.40
4	GND PWR		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
5	Sig2		Copper foil	1.0 oz	1.35
		4.3	Prepreg	1506+7628H	13.40
6	Sig3		Copper foil	1.0 oz	1.35
		3.7	Core	4mil	3.91
7	GND2		Copper foil	1.0 oz	1.35
		3.7	Prepreg	1080	2.40
8	Bottom		Copper foil	0.5oz	0.65
			Add Plating		1.30
			SolderMask		0.50
Overall Thickness (1.4mm ± 10%)				55.1	55.59000 1.411986

Reference GCE RD data

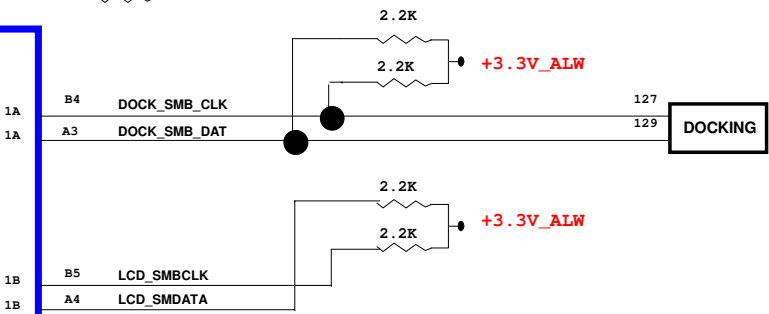
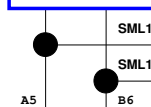
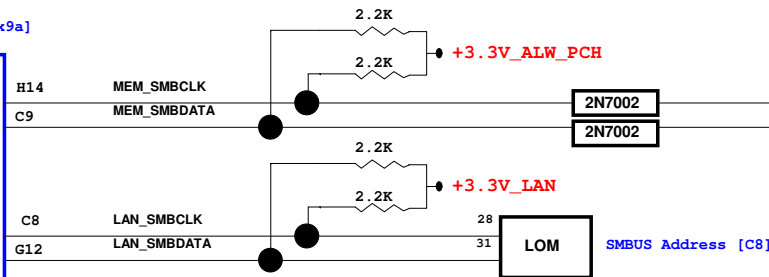
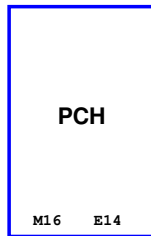
DSC DP/HDMI Port	Connetion
Port C	Dock DP port 2
Port D	Dock DP port 1
Port E	MB HDMI Conn

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Index and Config.			
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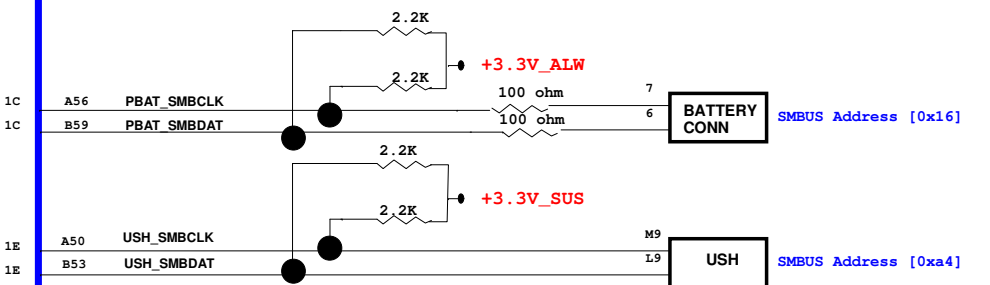
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SMBUS Address [0x9a]

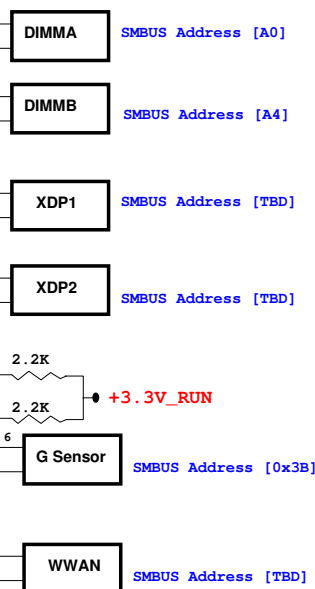
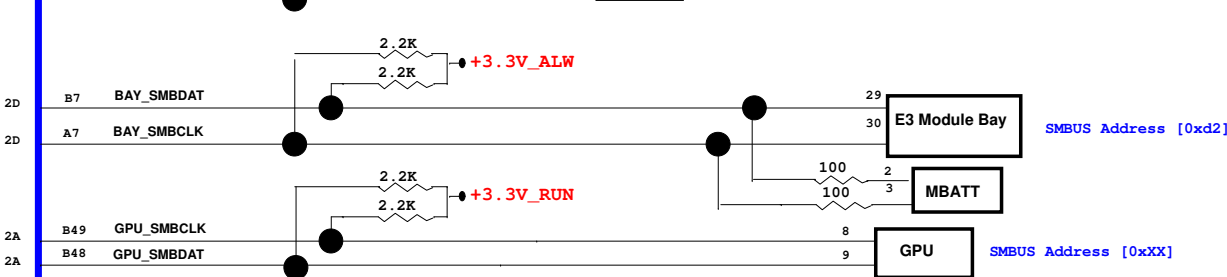
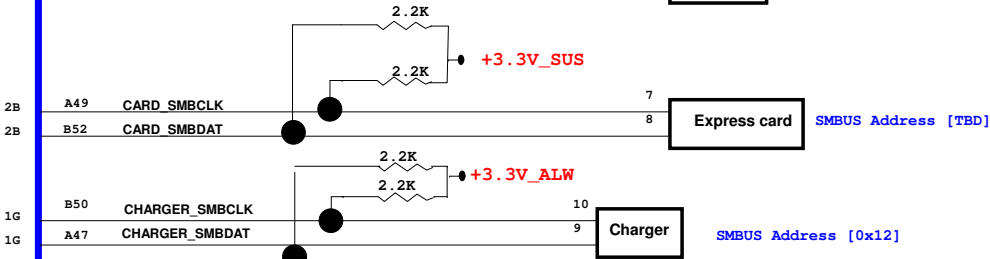


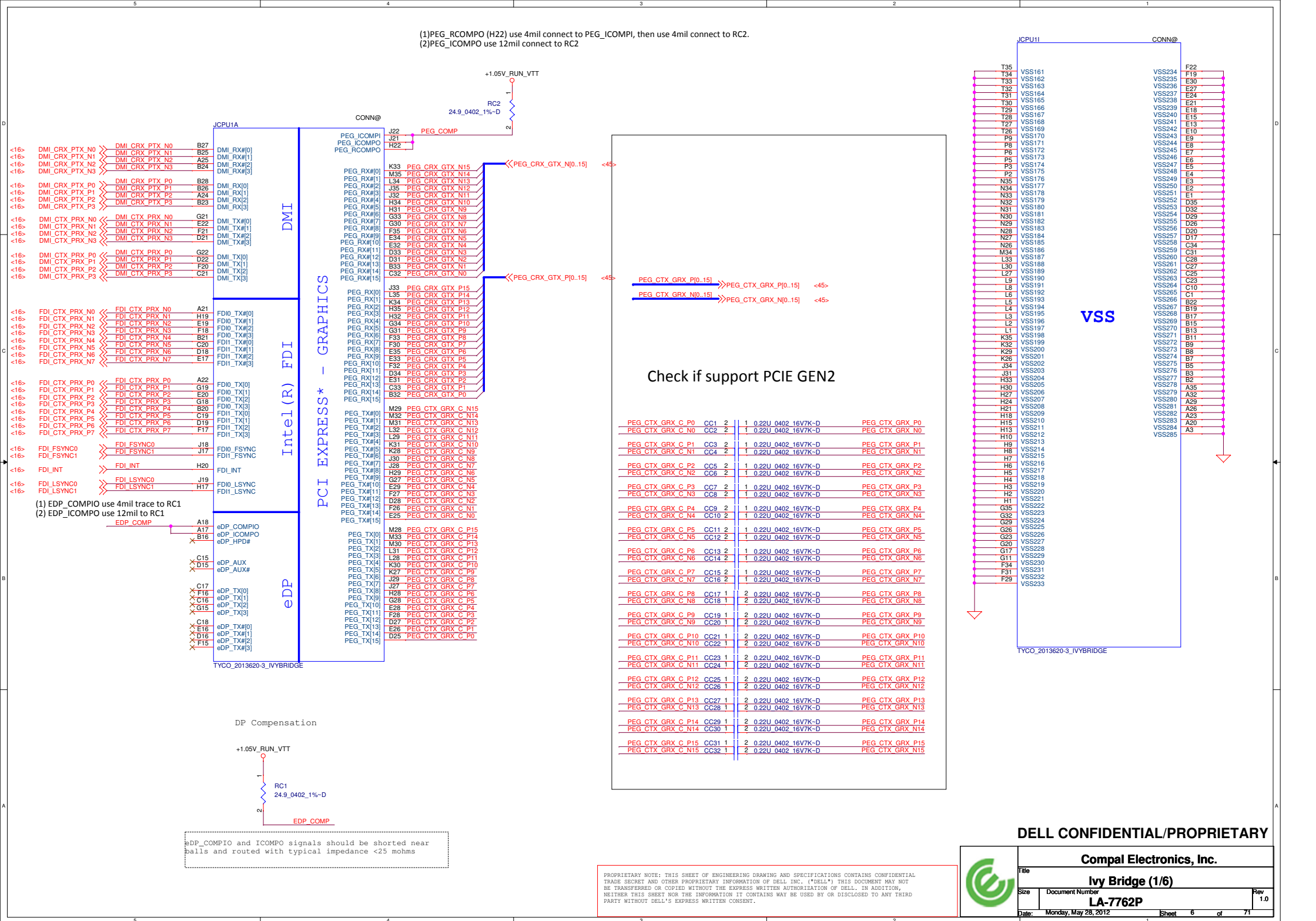
SMBUS Address
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SPR_EC: 0x70
MSLICE_EC: 0x72
USB: 0x59
AUDIO: 0x34
SLICE_BATTERY: 0x17
SLICE_CHARGER: 0x13

KBC

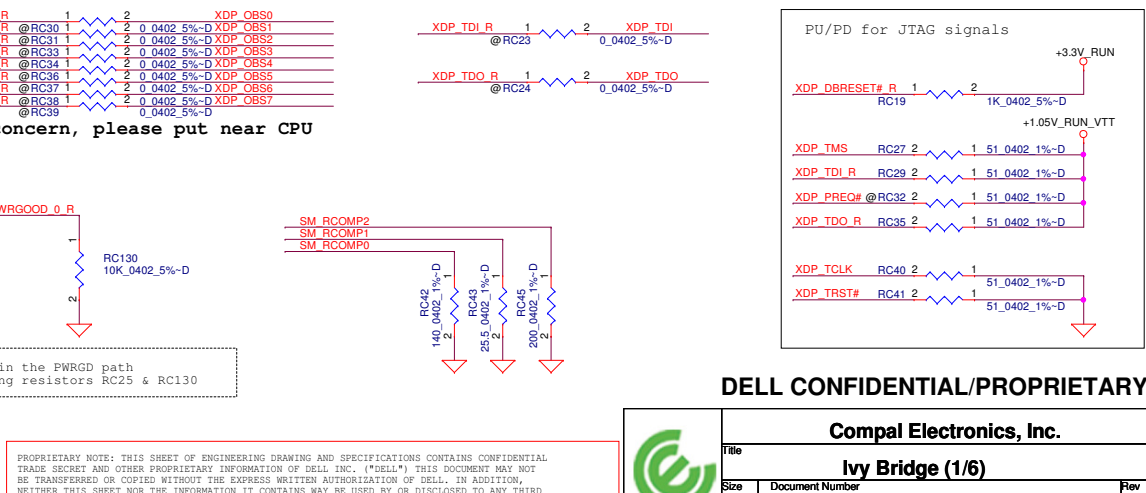
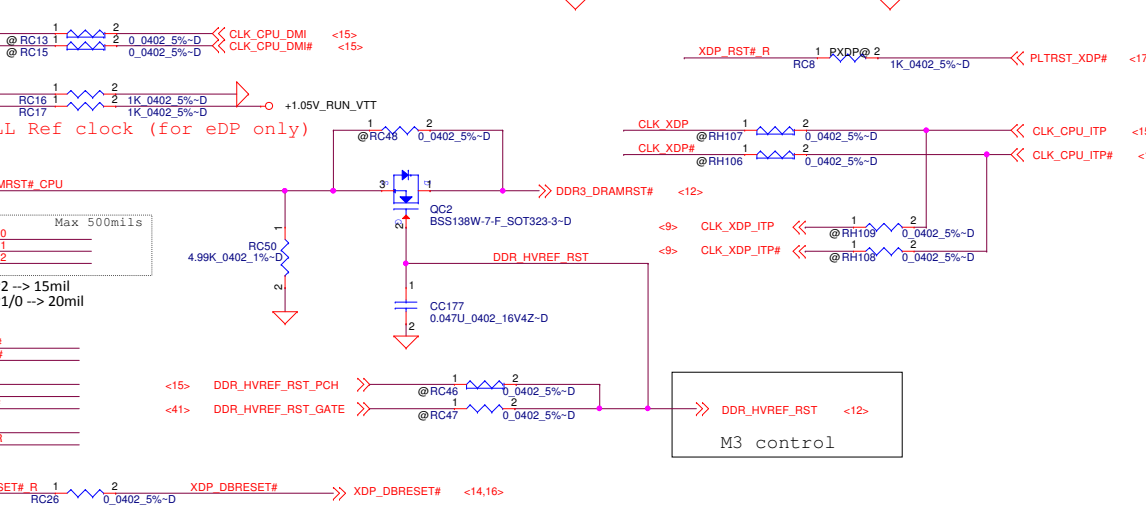
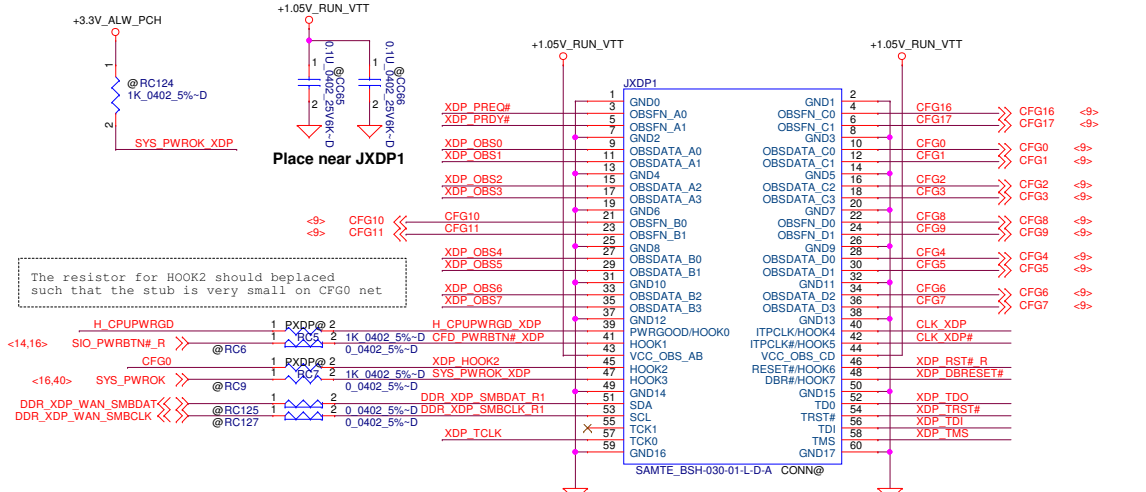
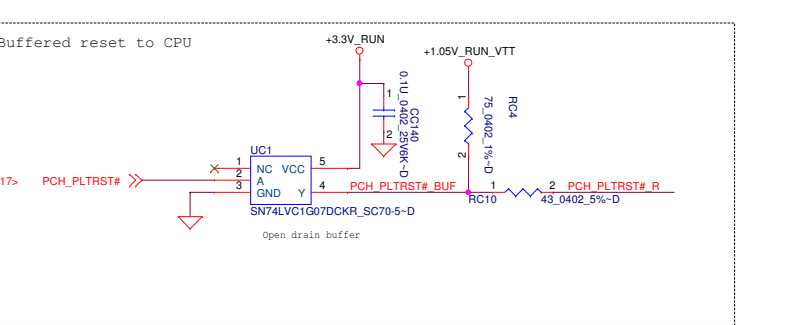
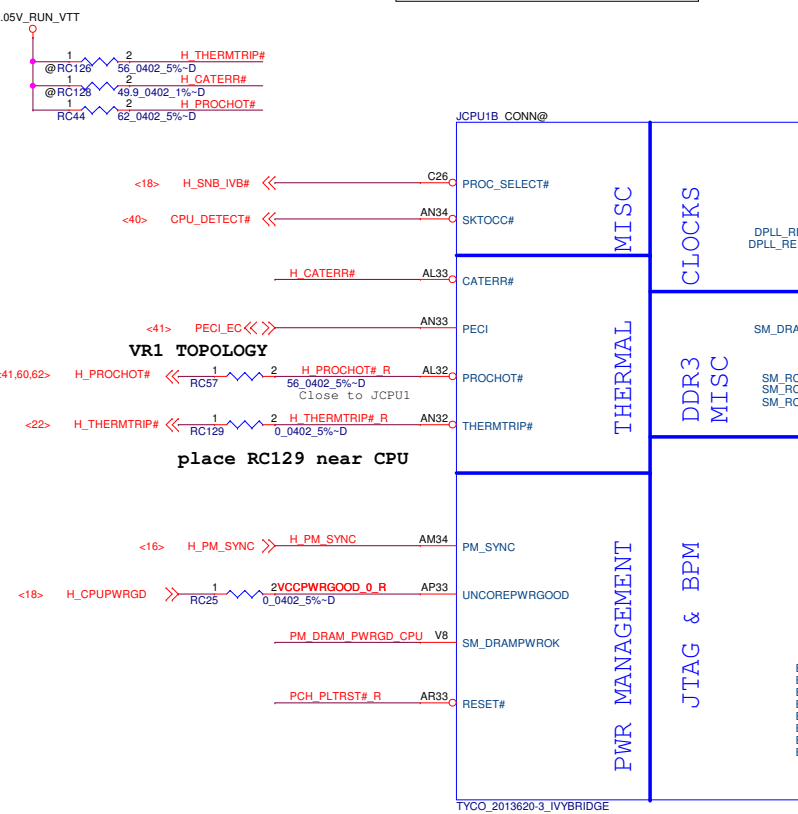
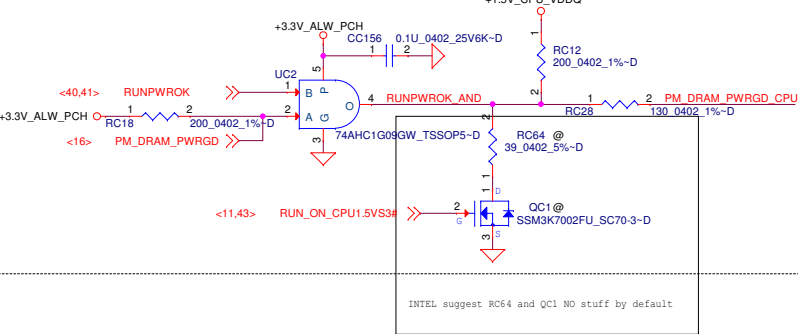


MEC 5055

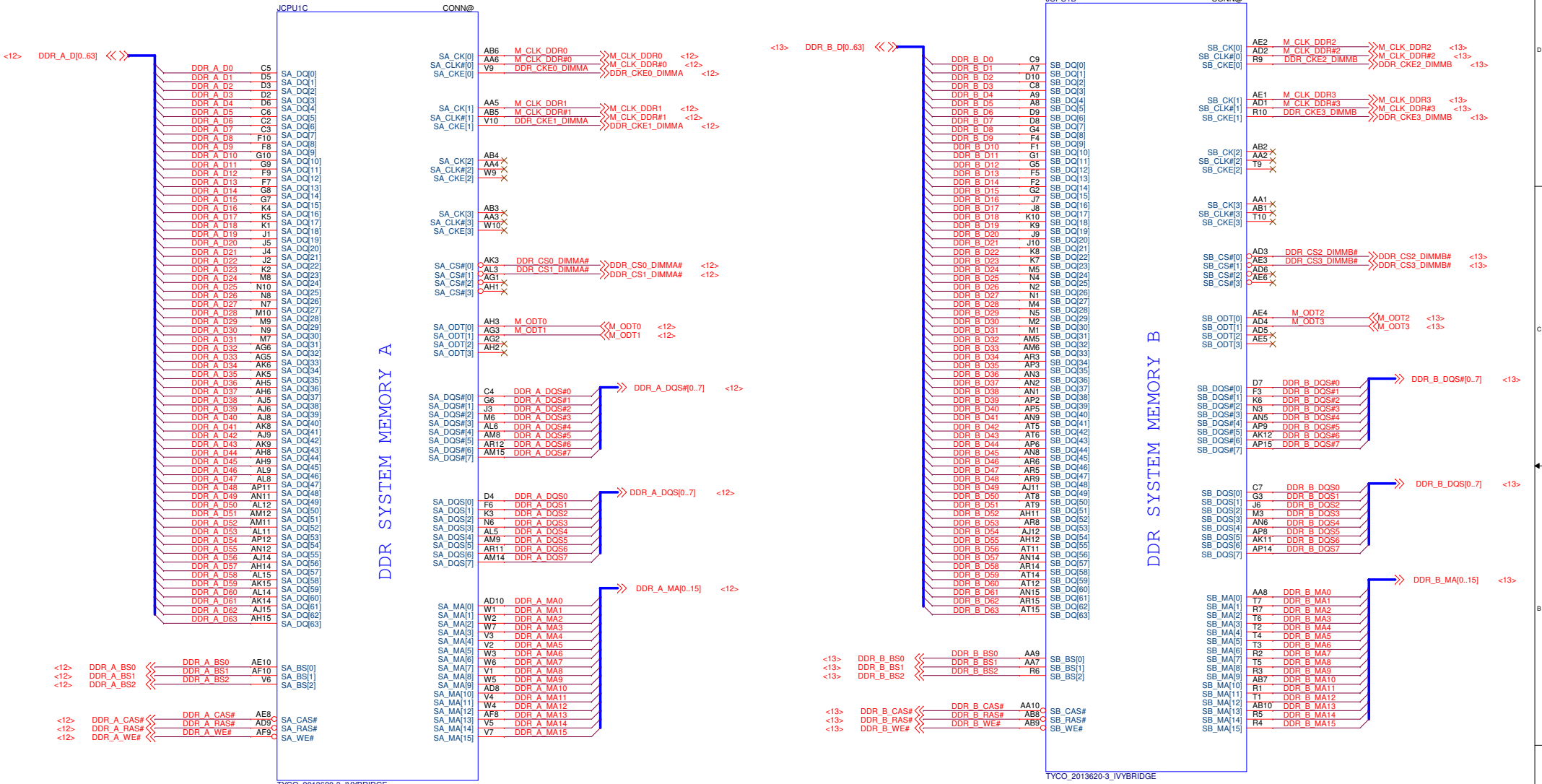




Follow DG Rev0.71 SM_DRAMPWROK topology



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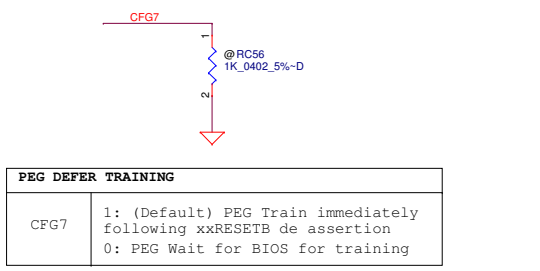
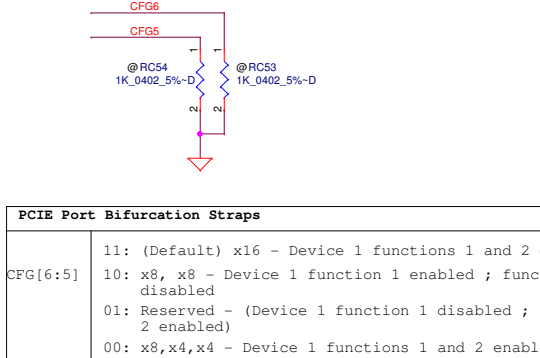
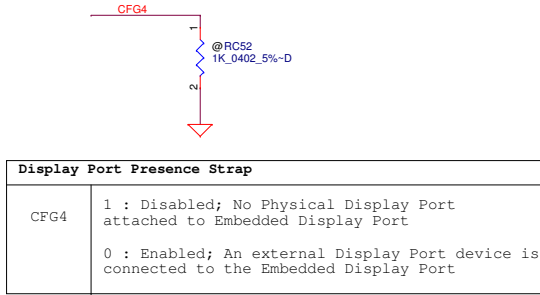
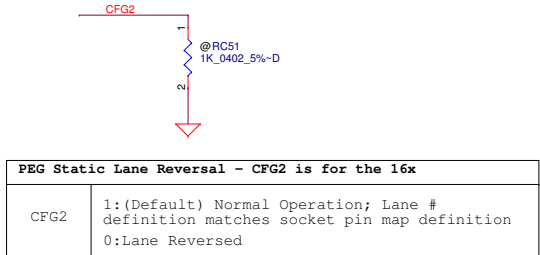
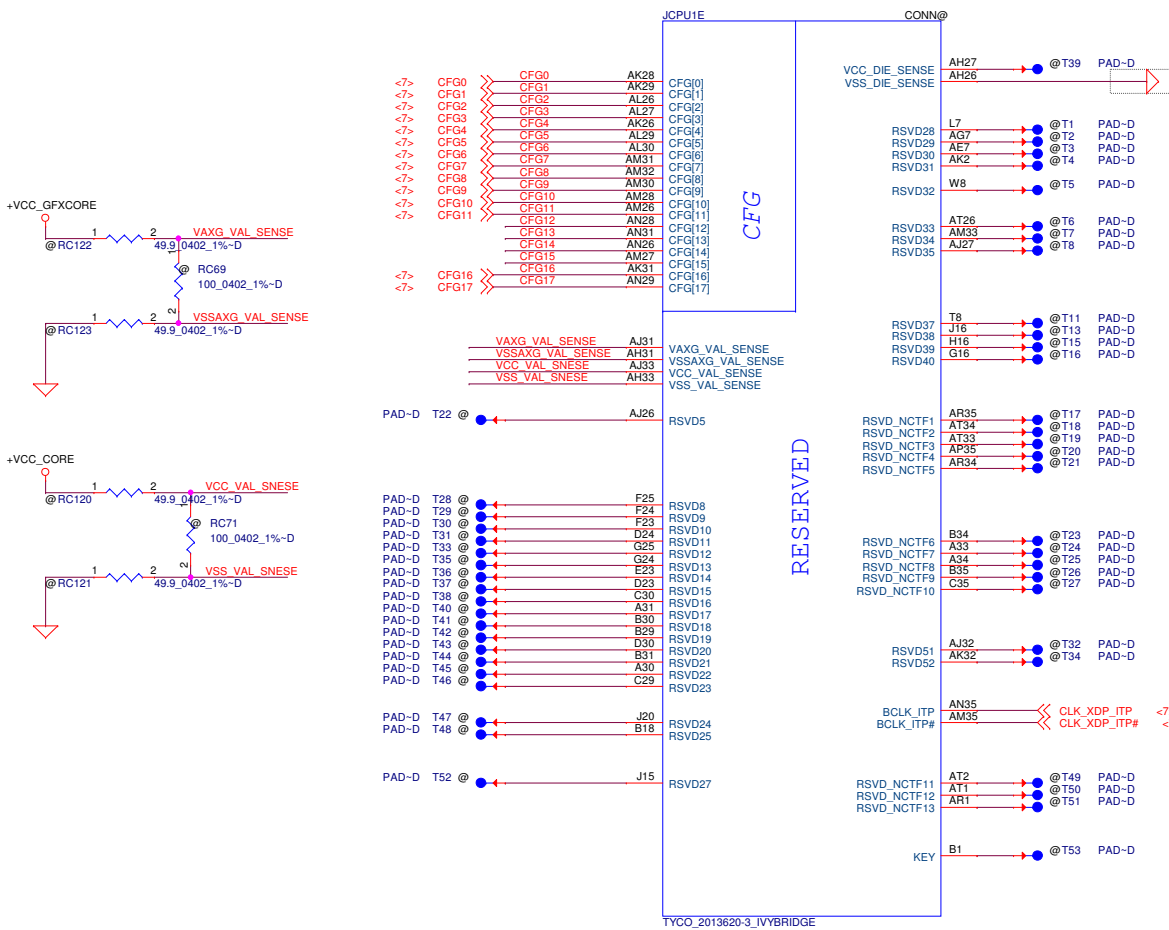


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CFG Straps for Processor

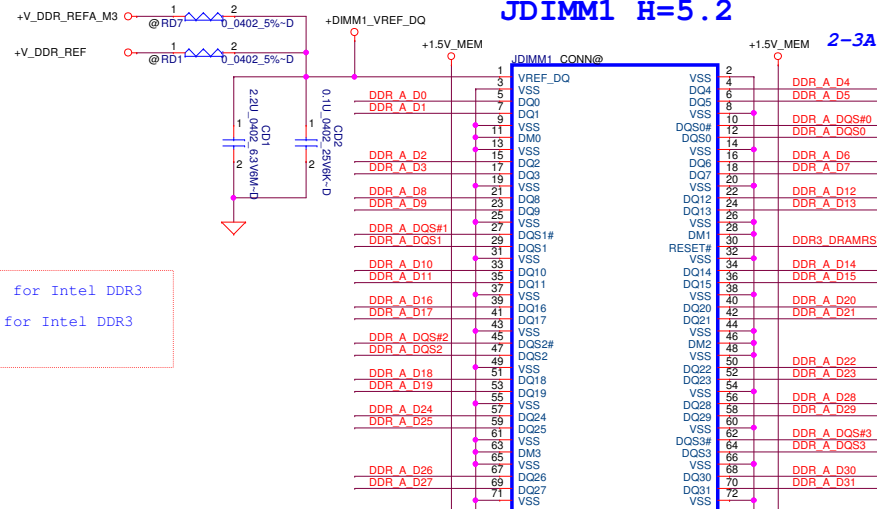


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JDIMM1 H=5.2

2-3A to 1 DIMMs/channel

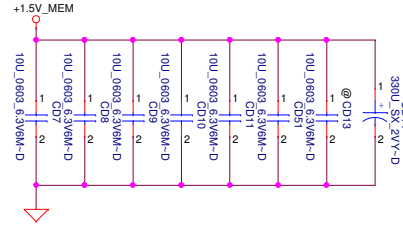
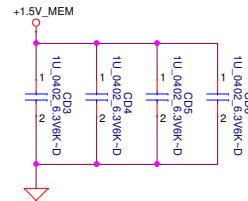


```
Populate RD1, De-Populate RD7  for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3
```

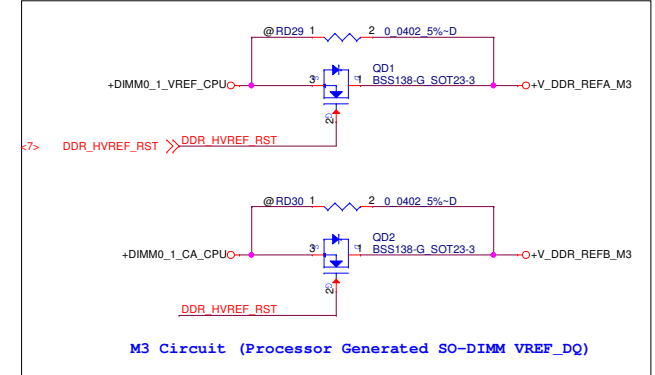
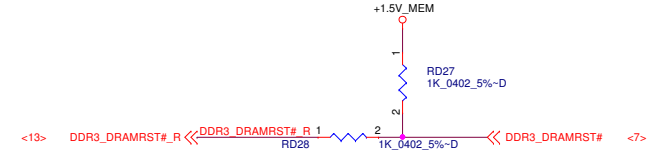
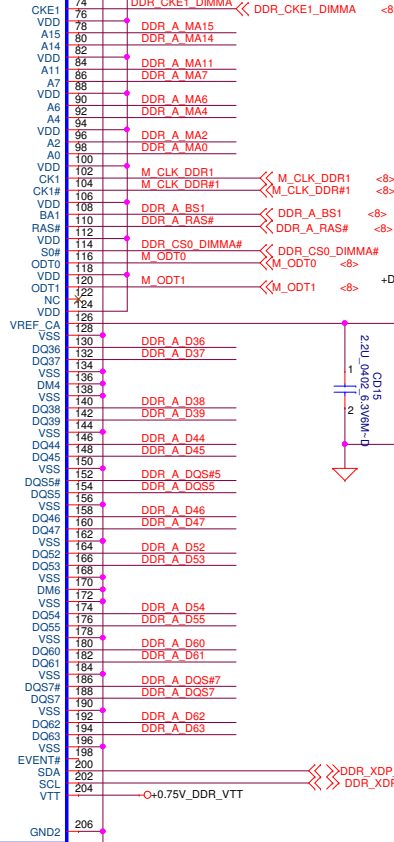
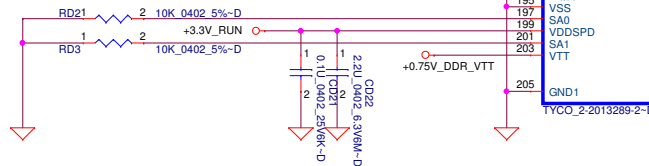
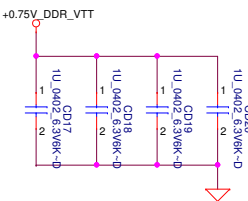
All VREF traces should
have 10 mil trace width



Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



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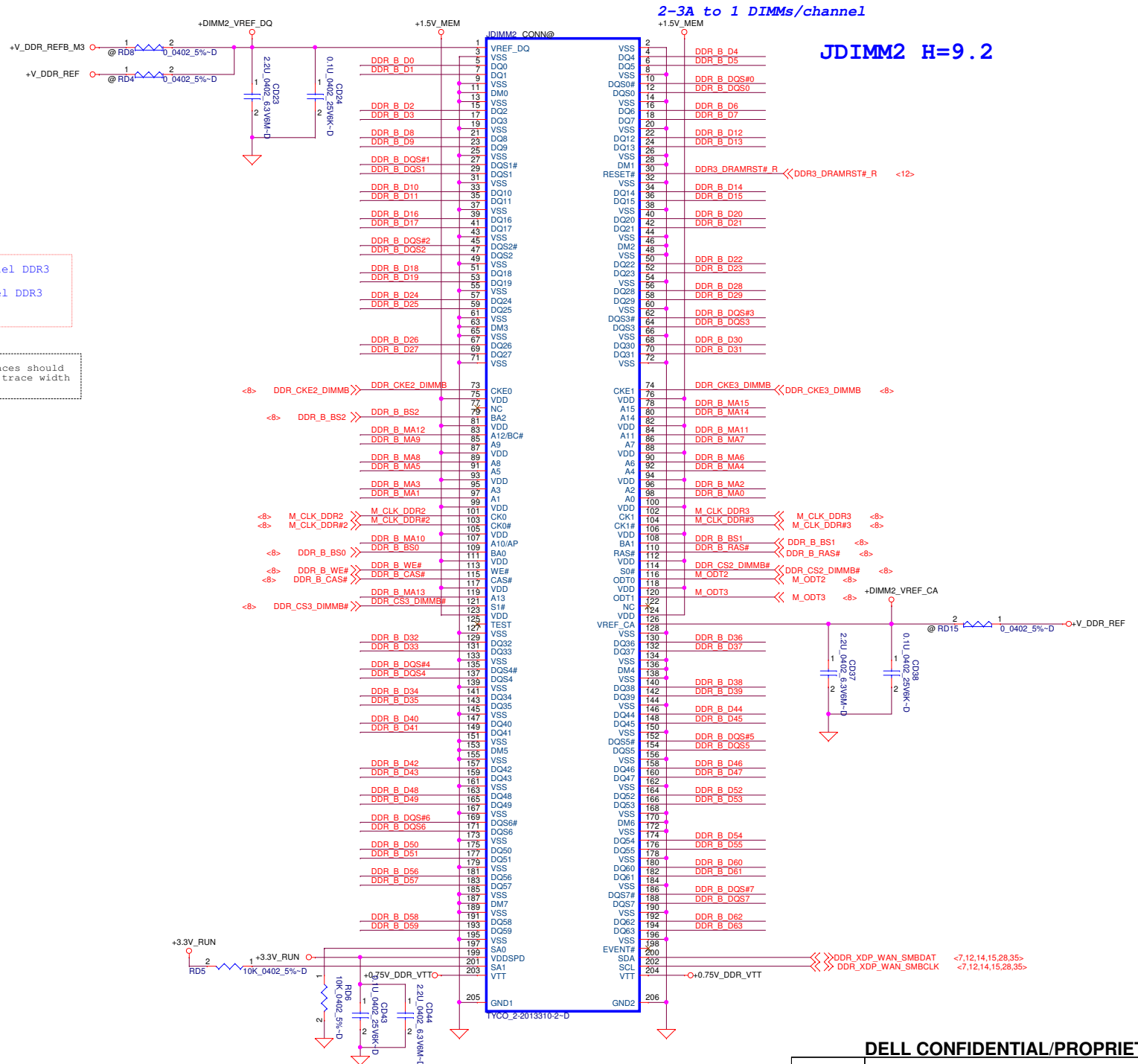
DDRIII-SODIMM SLOT1

LA-7762P

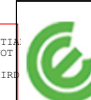
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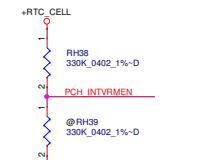


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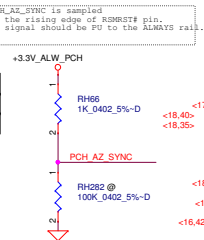
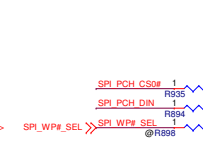
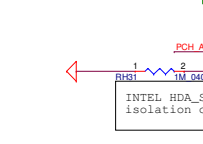
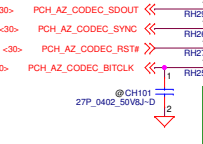
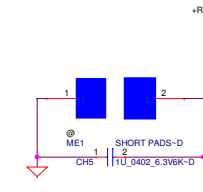


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DDR3-SODIMM SLOT2			
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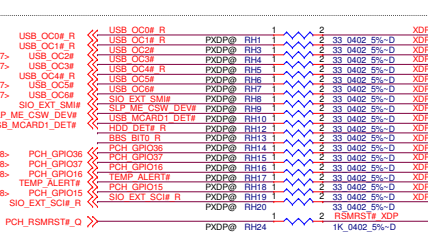
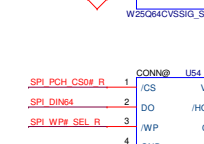
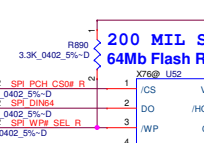
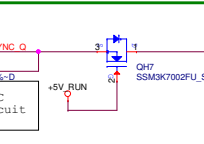
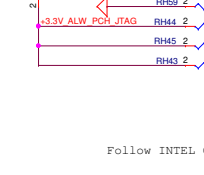
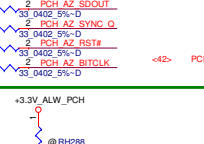
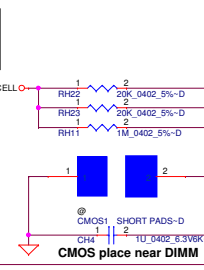
CMOS CLR1		CMOS setting	
Shunt	Clear CMOS	Open	Keep CMOS
ME CLR1		TPM setting	
Shunt	Clear ME RTC Registers	Open	Keep ME RTC Registers
Open	Keep CMOS	Open	Keep ME RTC Registers



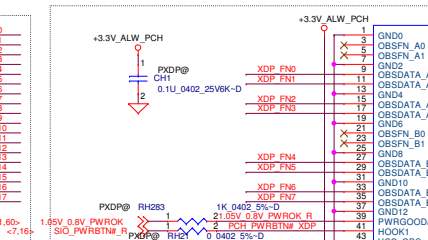
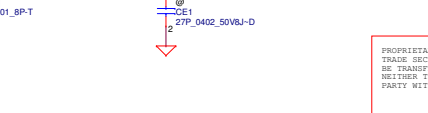
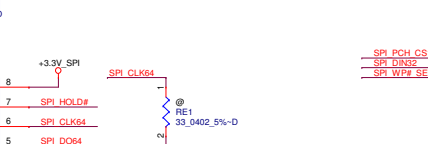
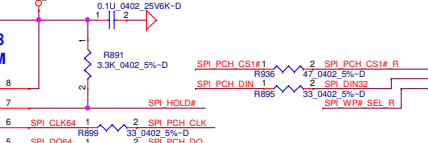
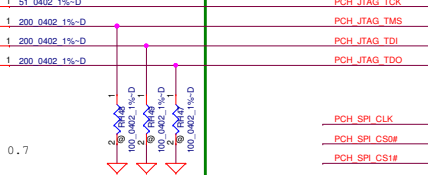
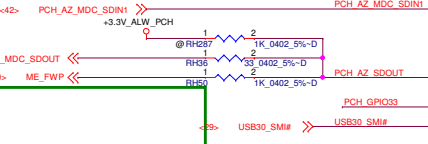
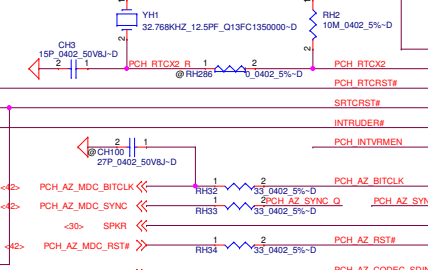
INTVRM - Integrated SUS
1.1V VRM Enable
High - Enable Internal VRs
Low - Enable External VRs



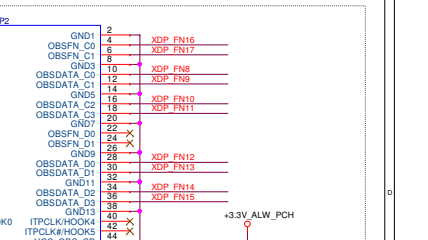
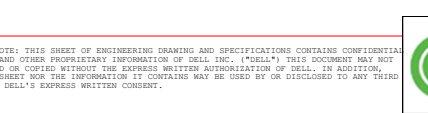
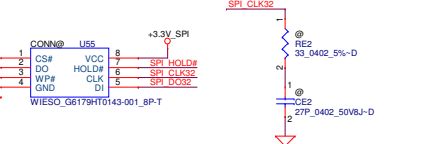
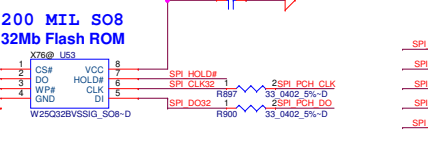
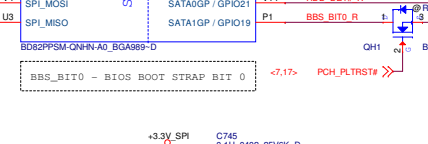
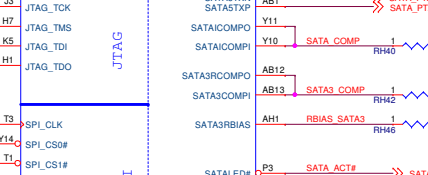
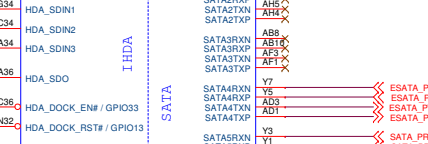
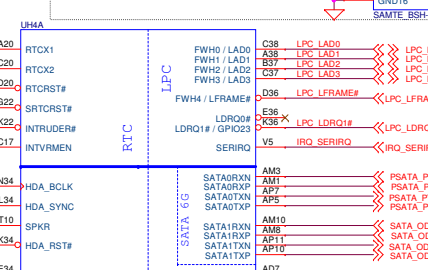
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



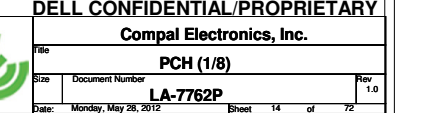
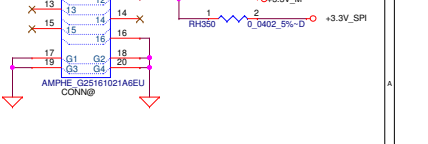
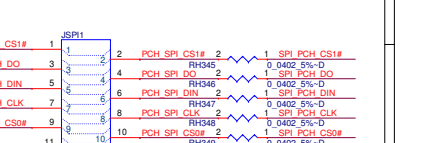
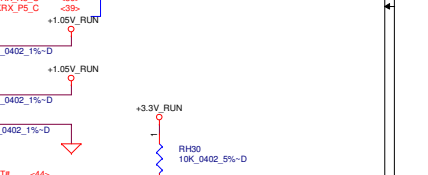
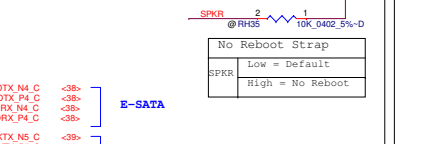
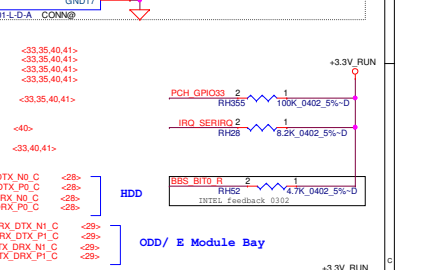
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low



On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low

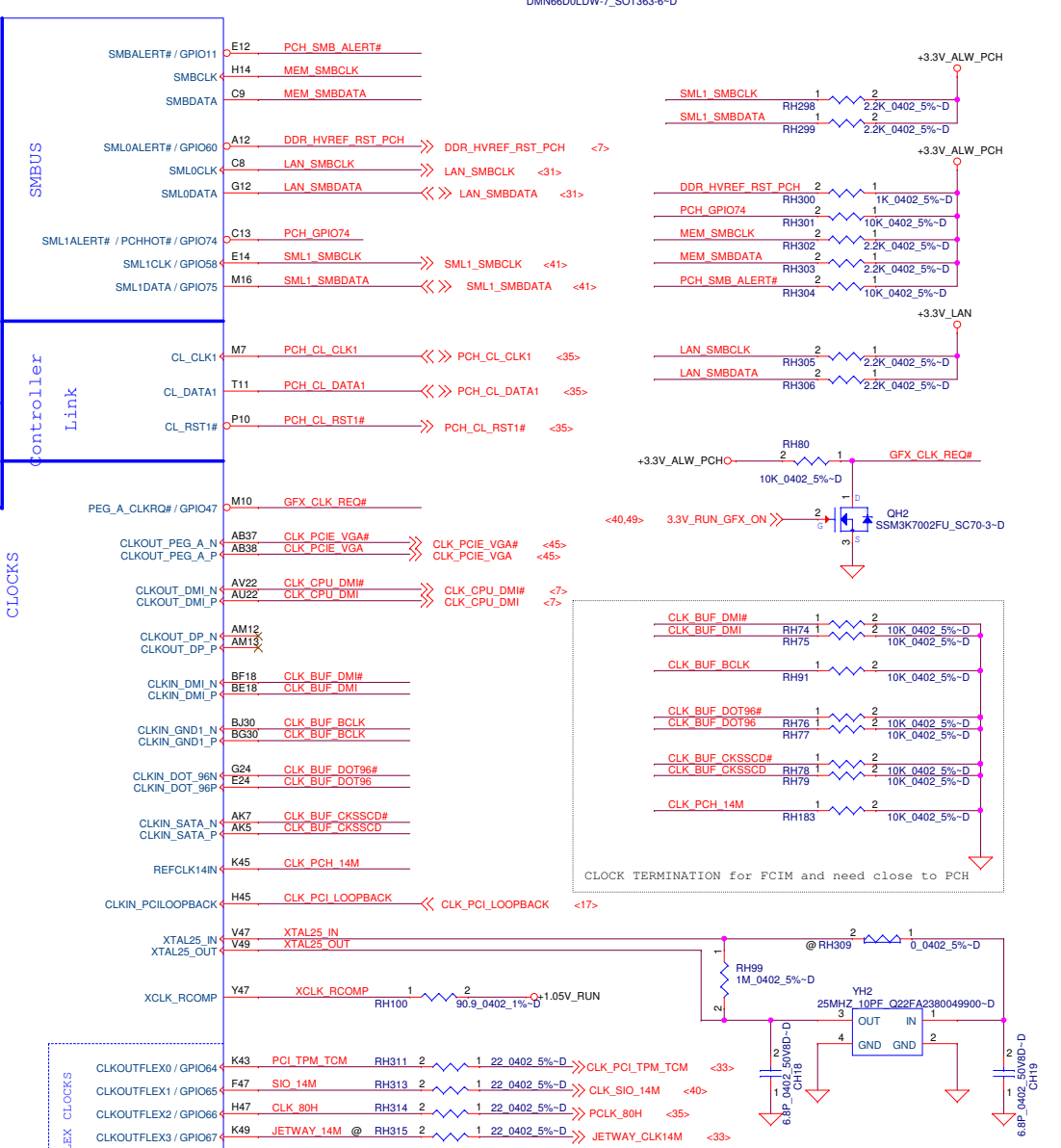
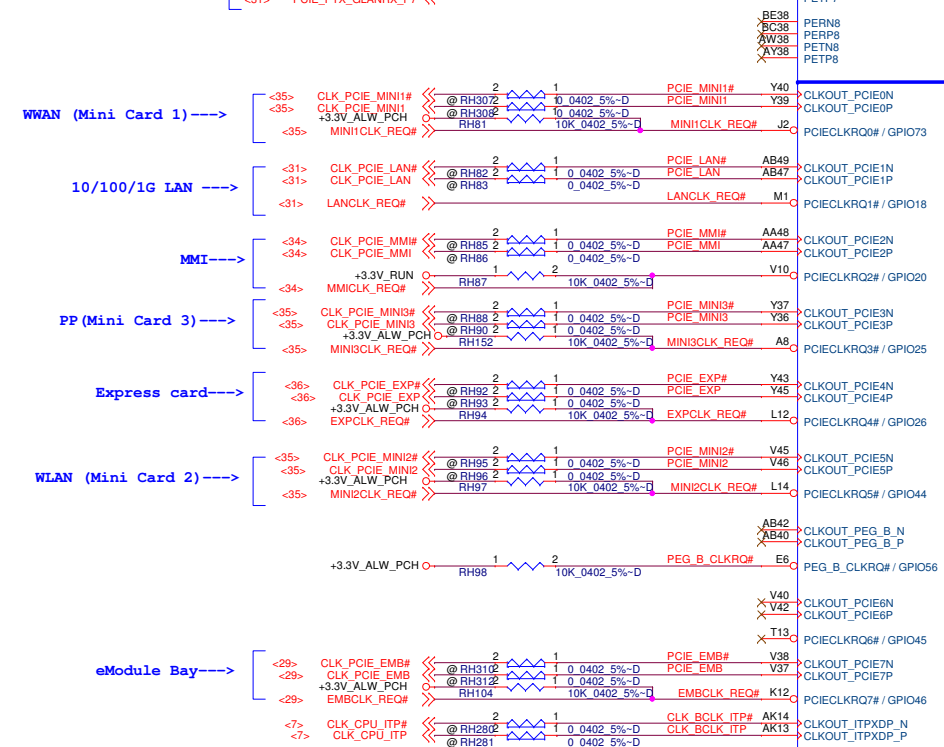
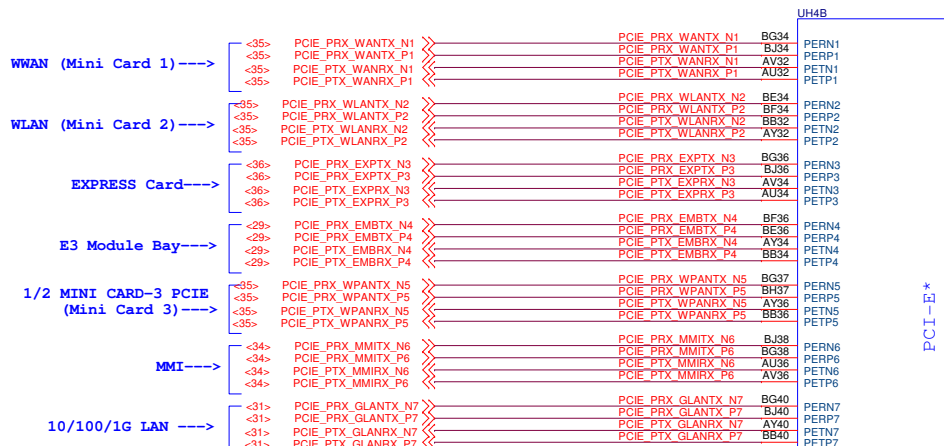


On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low




On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low





PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2

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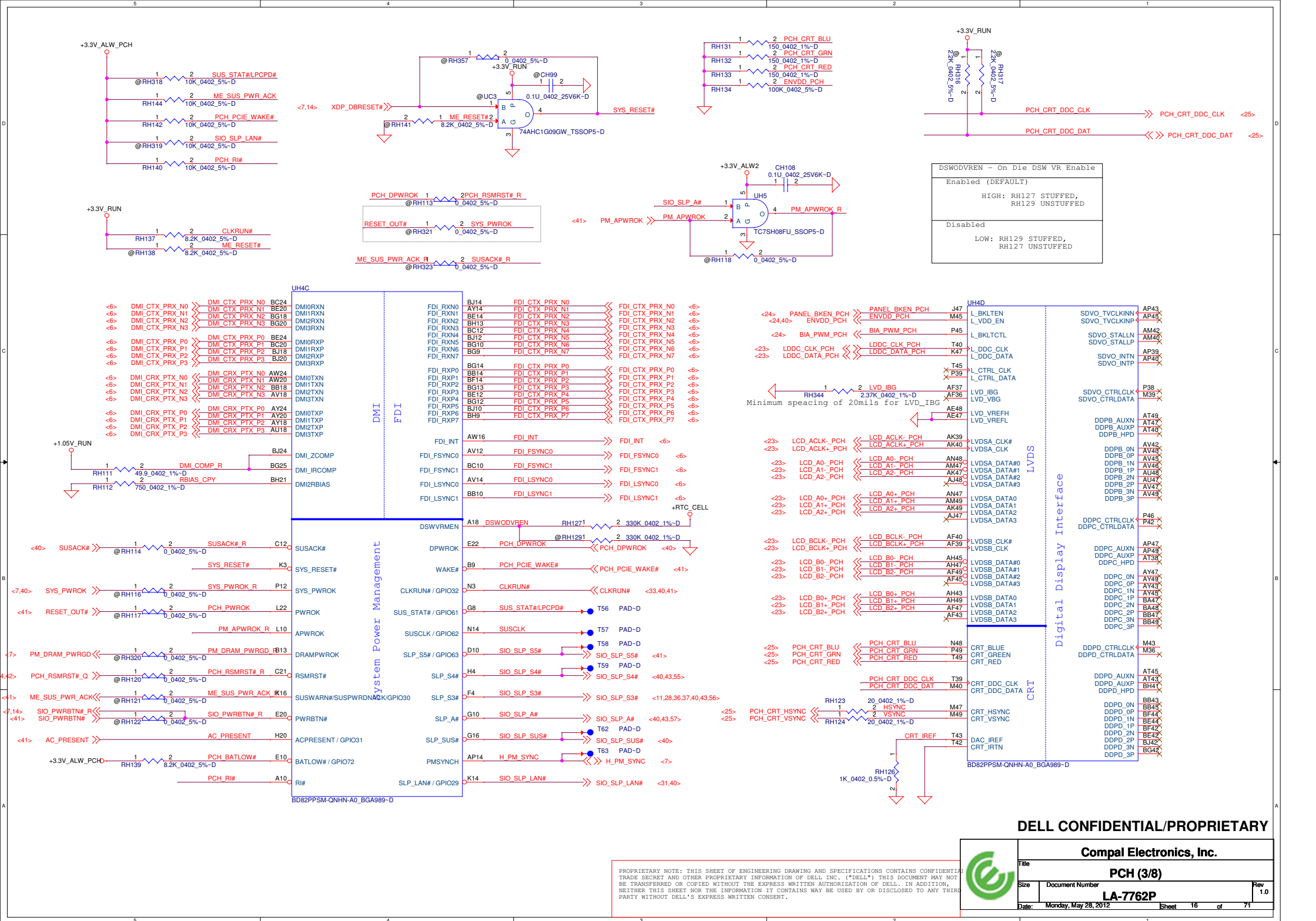
PCH (2/8)

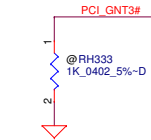
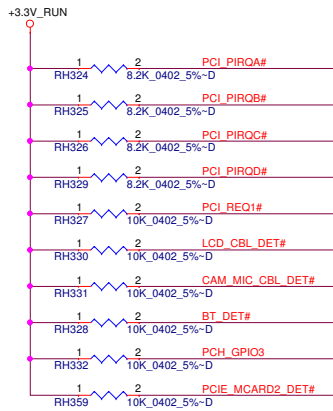
LA-7762P

Rev 1.0

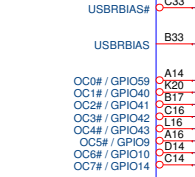
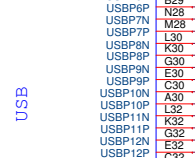
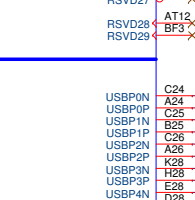
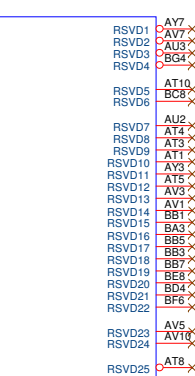
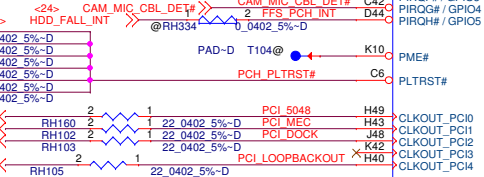
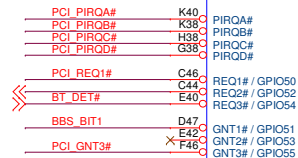
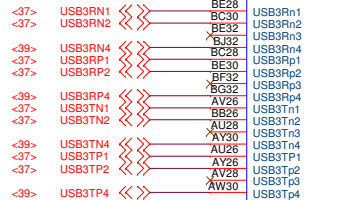
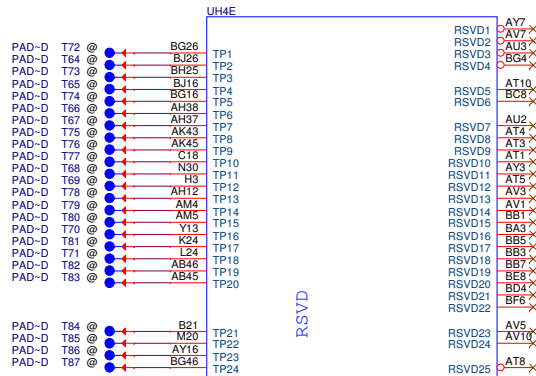
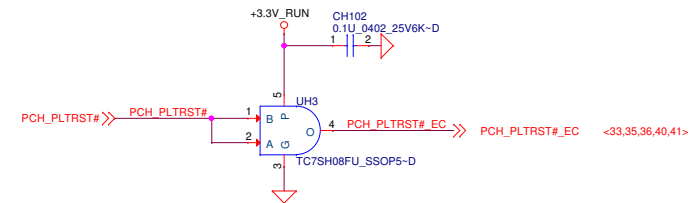
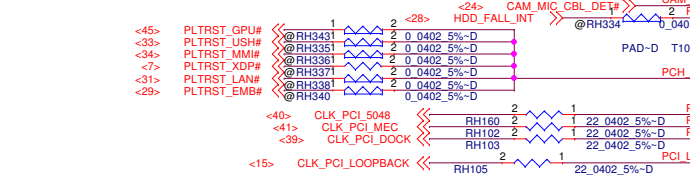
Monday, May 28, 2012

Sheet 15 of 71



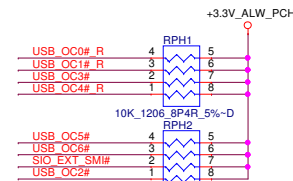


A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

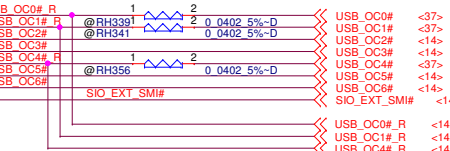


BD82PPSM-QNH-N-A0_BGA989-D

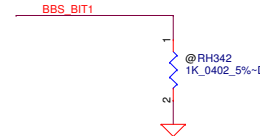
- >Right Side Top
- >Right Side Bottom
- >Right side E-SATA
- >MLK DOCK
- >WLAN/WIMAX
- >WWAN/UWB
- >DOCK
- >USH
- >Flash
- >Left side
- >Express Card
- >Blue Tooth
- >Camera
- >LCD Touch

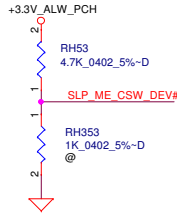


Trace width 4mil,space15 mils,within 500 mils.



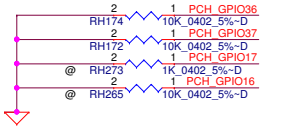
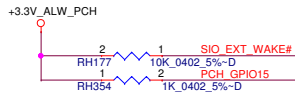
Boot BIOS Strap		
BBS_BIT1	SATA_SLDP (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI



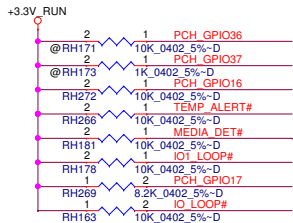


Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET# (GPIO27)

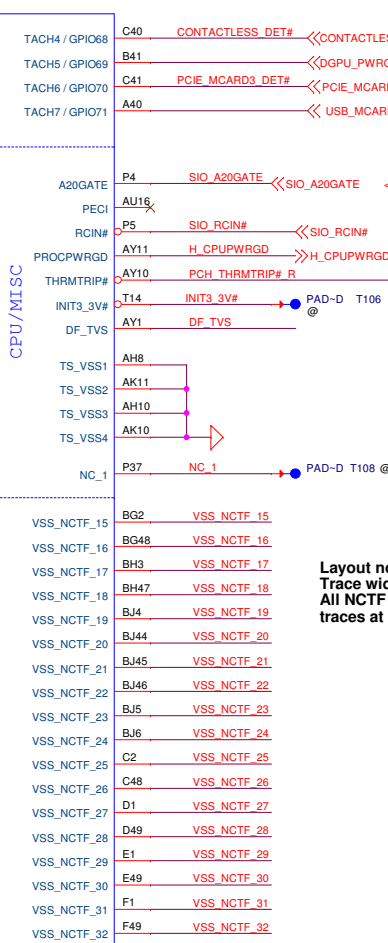
SLP_ME_CSW_DEV#	PLL ON DIE VR ENABLE
ENABLED - HIGH DEFAULT	
DISABLED - LOW	



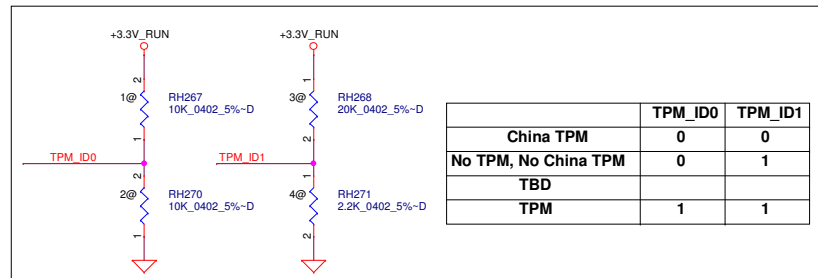
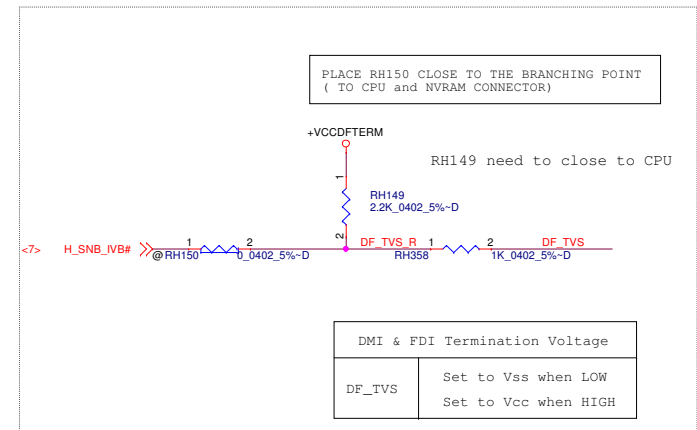
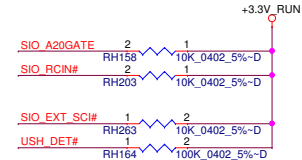
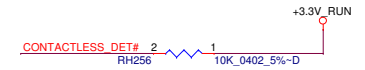
Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



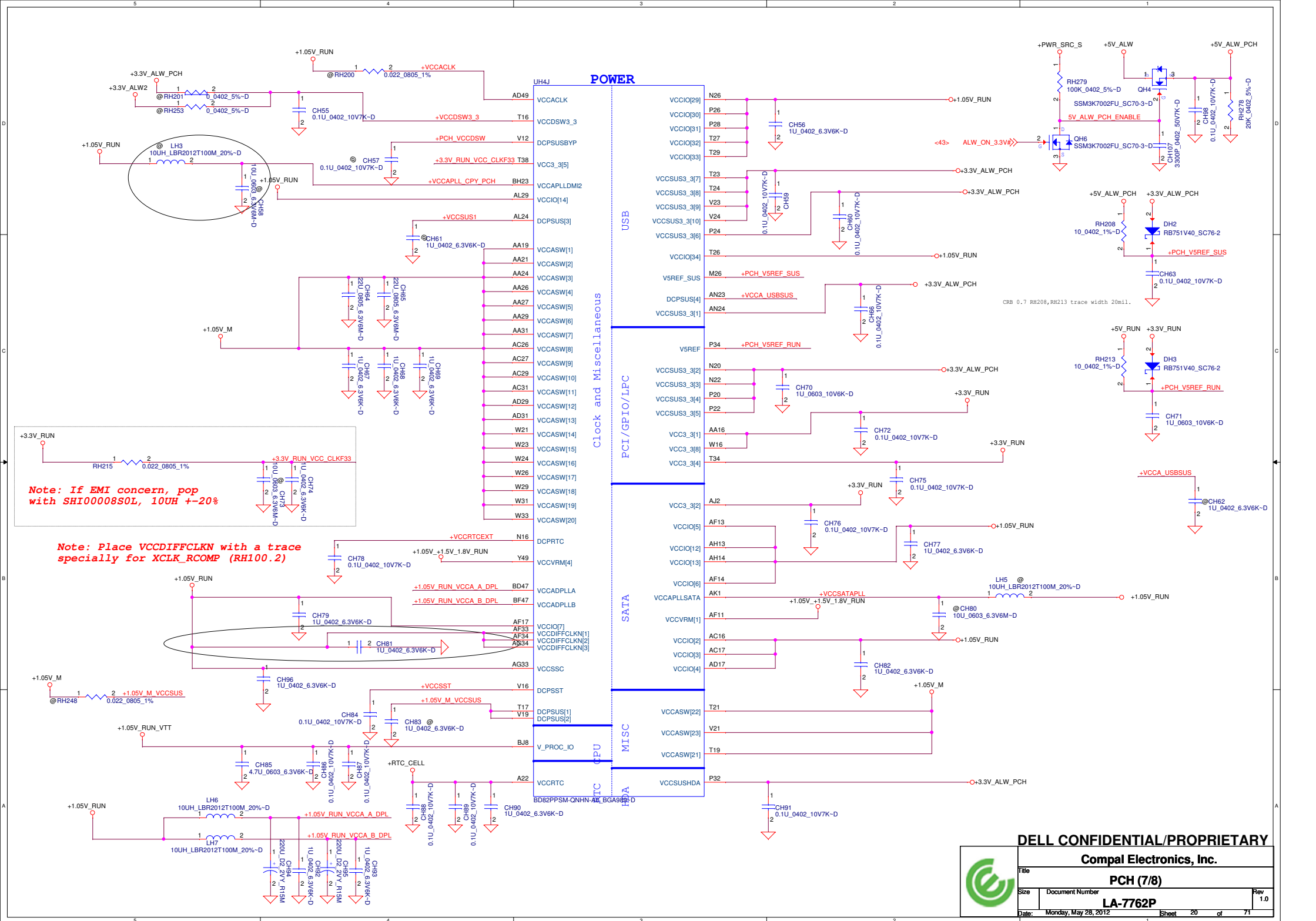
VSS_NCTF_1	A4	VSS_NCTF_1
VSS_NCTF_2	A44	VSS_NCTF_2
VSS_NCTF_3	A45	VSS_NCTF_3
VSS_NCTF_4	A46	VSS_NCTF_4
VSS_NCTF_5	A5	VSS_NCTF_5
VSS_NCTF_6	A6	VSS_NCTF_6
VSS_NCTF_7	B3	VSS_NCTF_7
VSS_NCTF_8	B47	VSS_NCTF_8
VSS_NCTF_9	BD1	VSS_NCTF_9
VSS_NCTF_10	BD49	VSS_NCTF_10
VSS_NCTF_11	BE1	VSS_NCTF_11
VSS_NCTF_12	BE49	VSS_NCTF_12
VSS_NCTF_13	BF1	VSS_NCTF_13
VSS_NCTF_14	BF49	VSS_NCTF_14

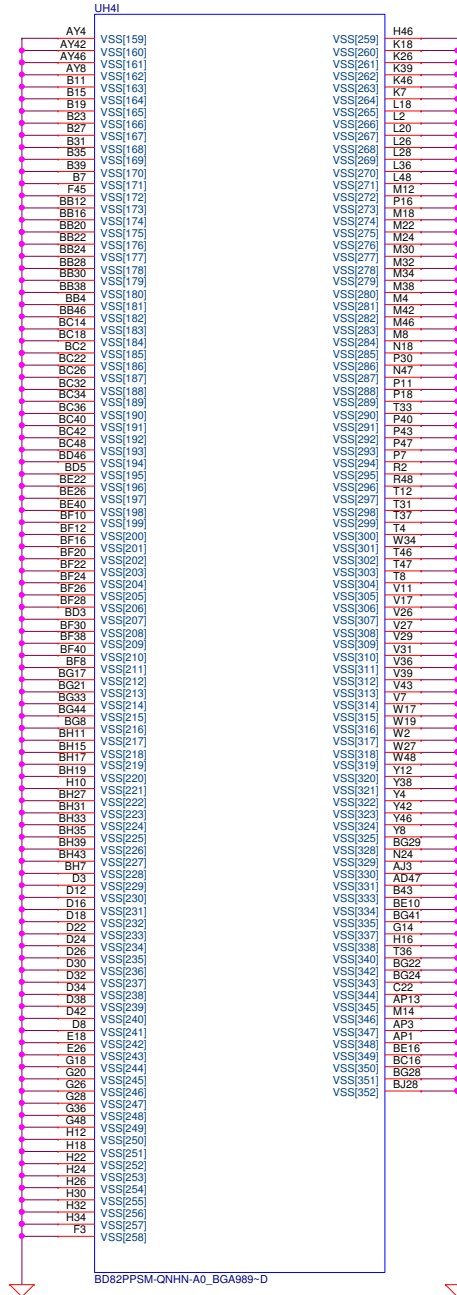
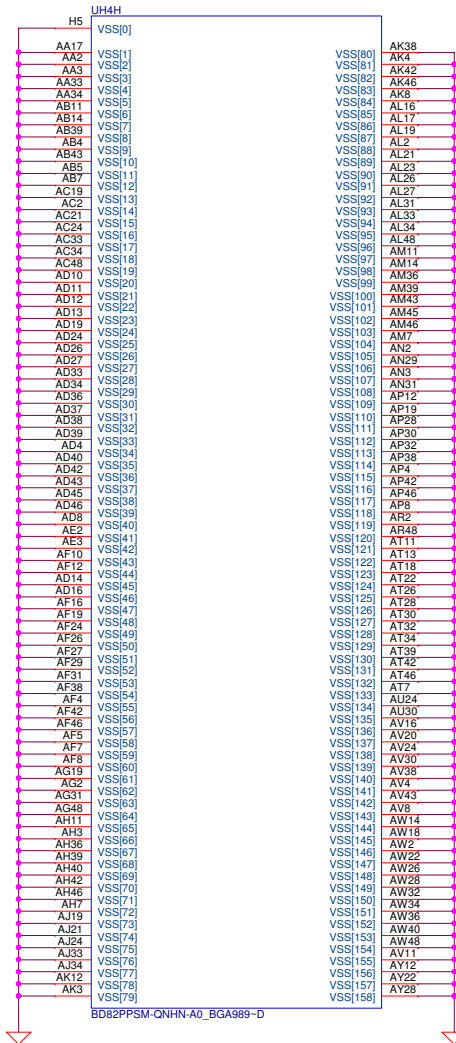


Layout note:
Trace wide 10mil & length 30mil
All NCTF pins should have thick traces at 45° from the pad.



	TPM_ID0	TPM_ID1
China TPM	0	0
No TPM, No China TPM	0	1
TBD		
TPM	1	1





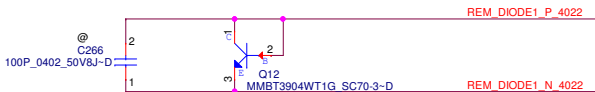
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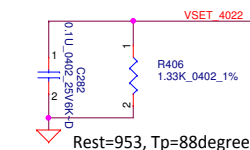
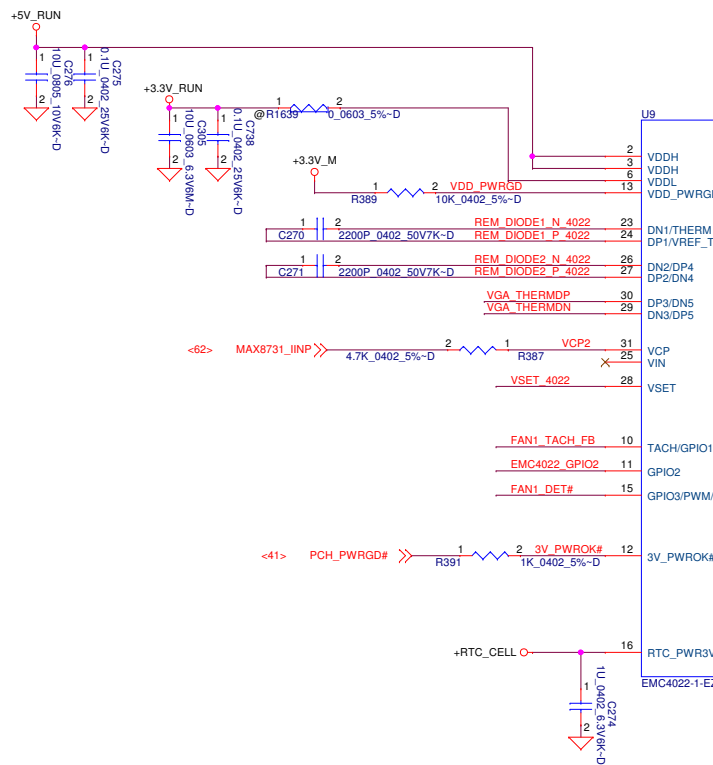
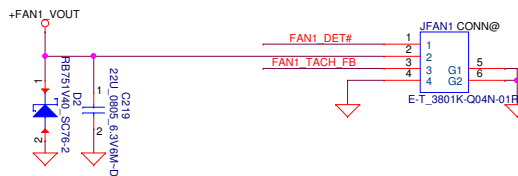
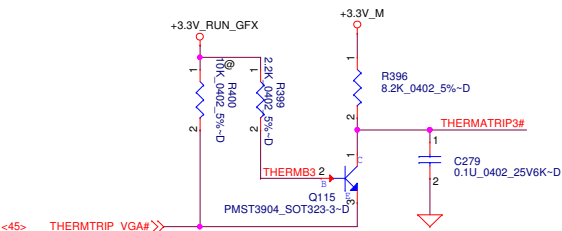
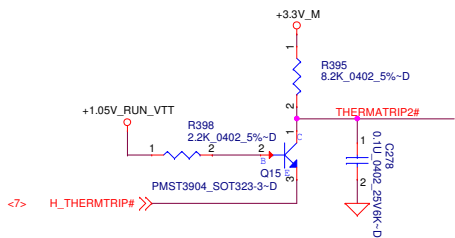
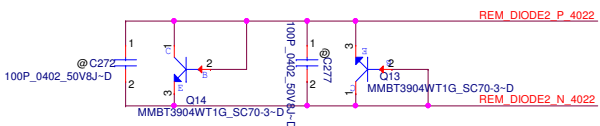
Title				PCH (8/8)	
Size				Document Number	Rev
				LA-7762P	1.0
Date				Monday, May 28, 2012	Sheet 21 of 71

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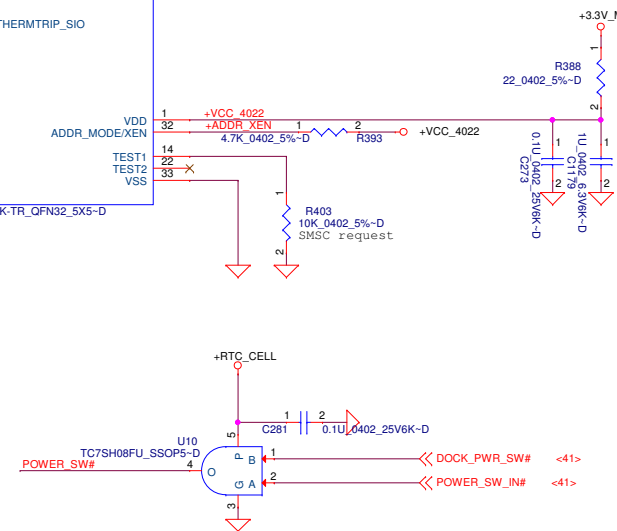
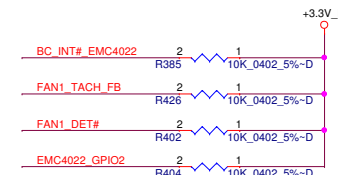
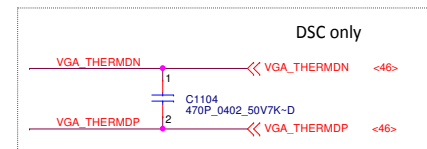
Place under CPU
Place C266 close to the Q12 as possible



- (1) DP2/DN2 for SODIMM on Q14, place Q14 close to SODIMM and C272 close to Q14
- (2) DP4/DN4 for Skin on Q13, place Q13 close to Vcore VR choke.



Rest=953, Tp=88degree

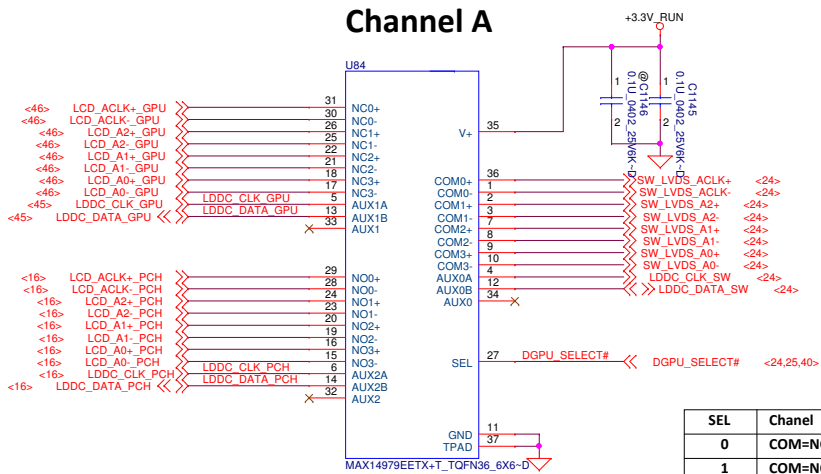


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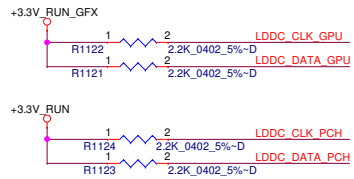
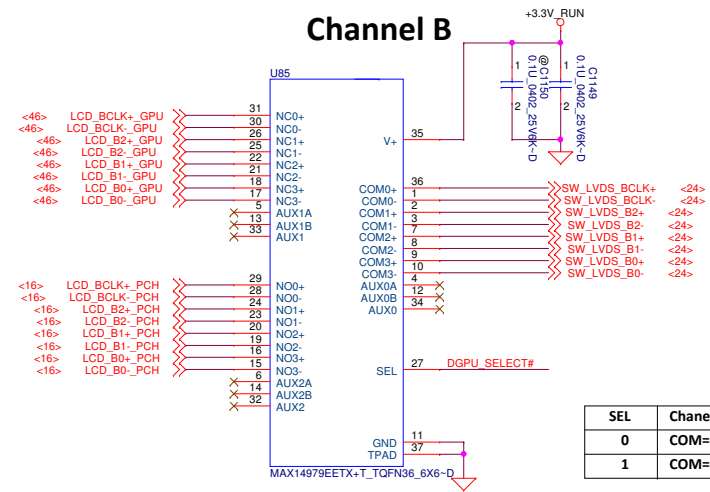
Compal Electronics, Inc.			
Title	FAN & Thermal Sensor		
Size	Document Number	Rev	
	LA-7762P	1.0	
Date:	Monday, May 28, 2012	Sheet	22 of 71

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Channel A



Channel B

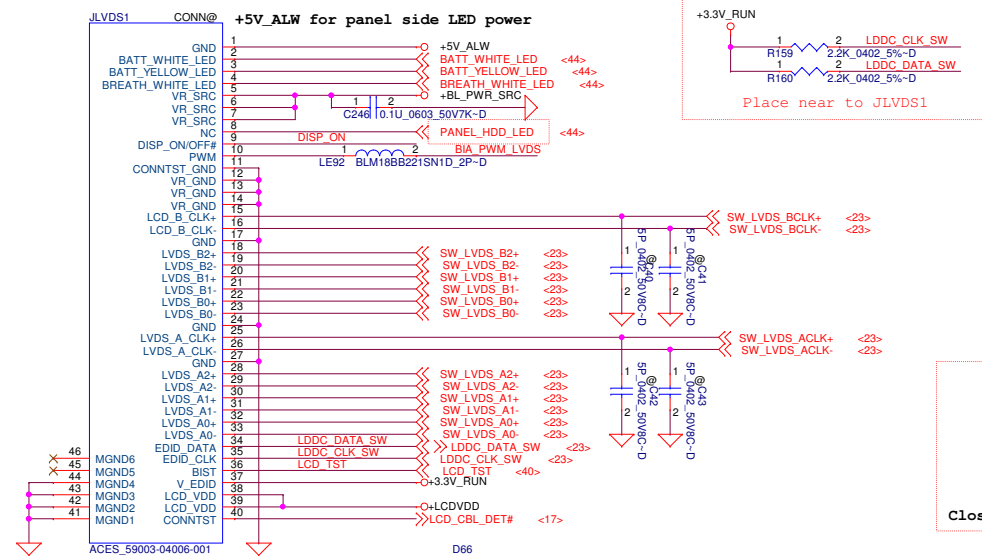


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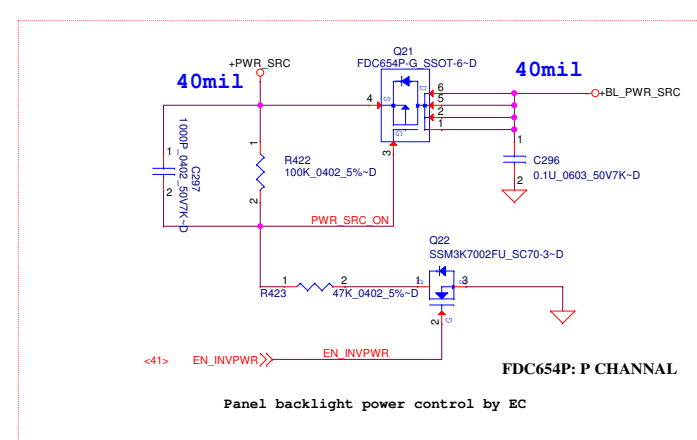
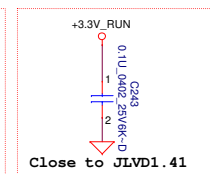
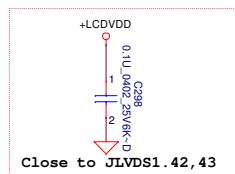
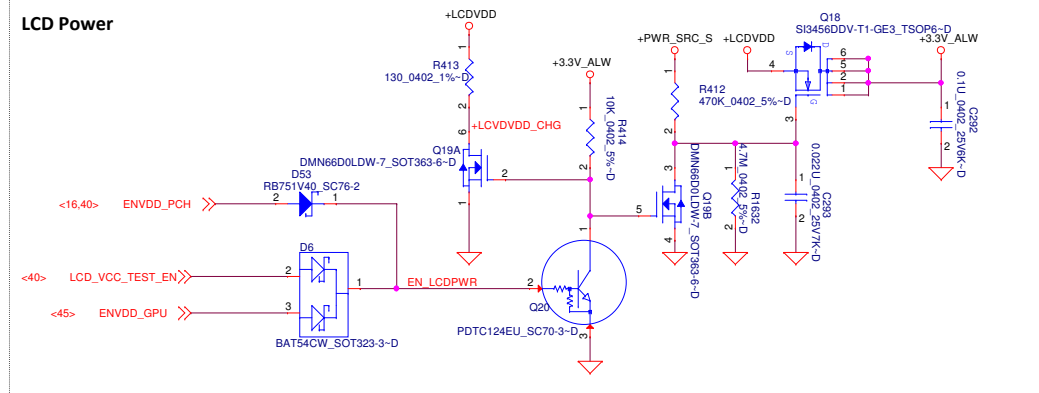
Compal Electronics, Inc.

Title			LA-7762P
Size			Rev 1.0
Date: Monday, May 28, 2012			Sheet 23 of 71

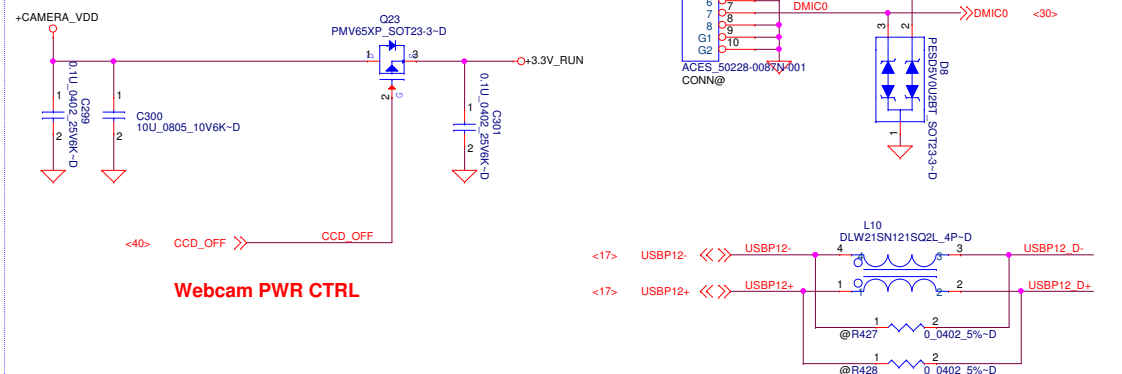
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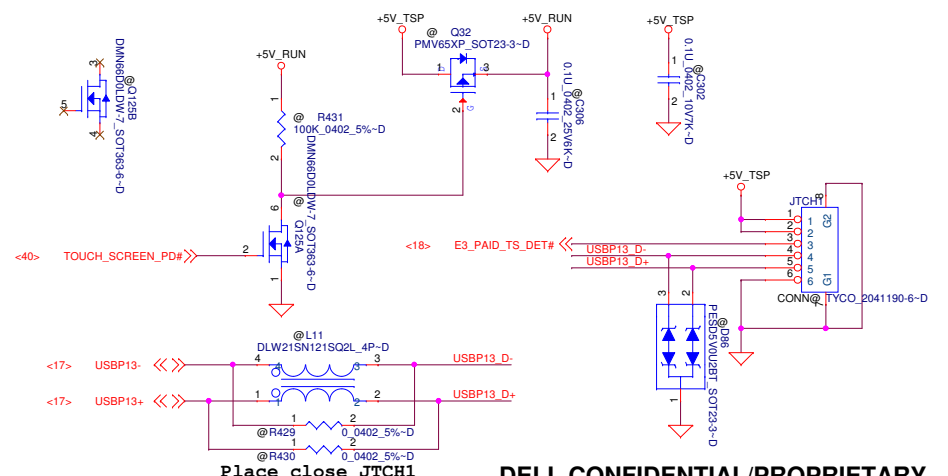
LCD Power



For Webcam



Touch Screen Connector



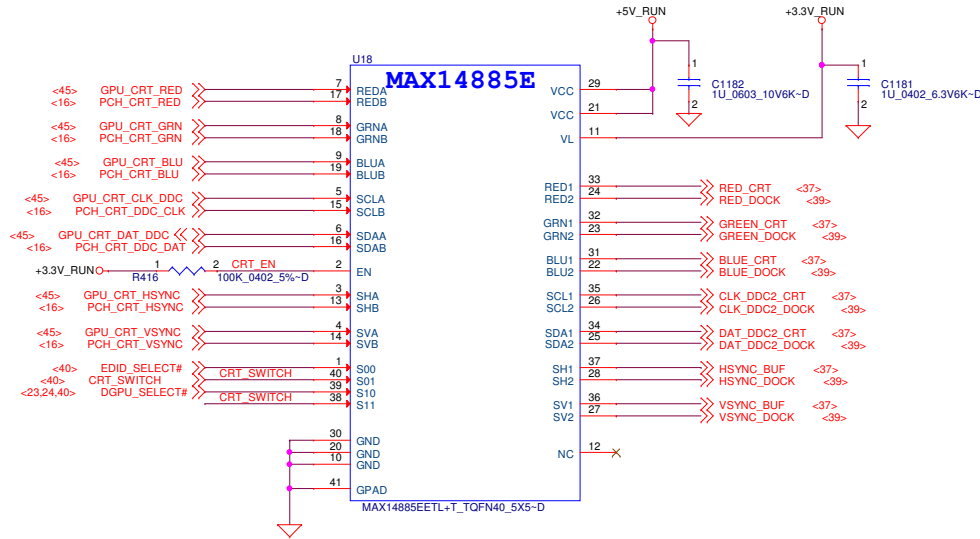
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Compal Electronics, Inc.			
eDP & CAM & TS Conn			
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Date:	Monday, May 28, 2012	Sheet	24 of 71

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Channel A --> GPU

Channel B --> PCH

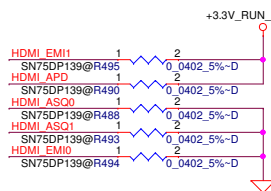
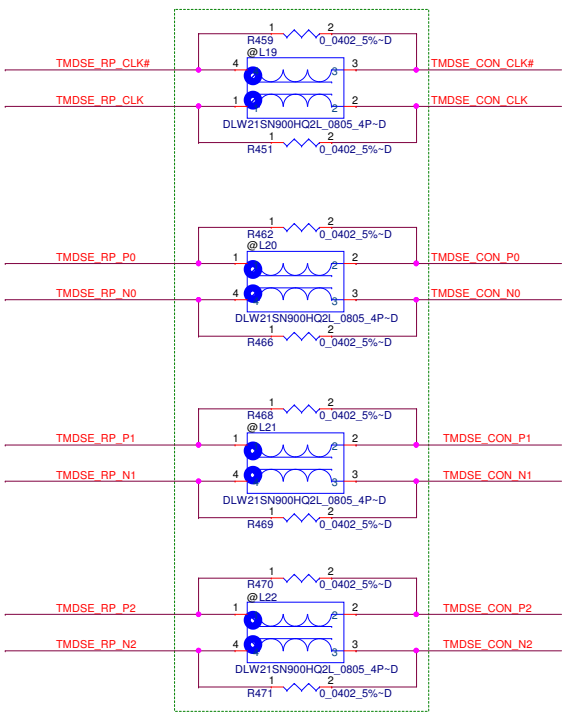
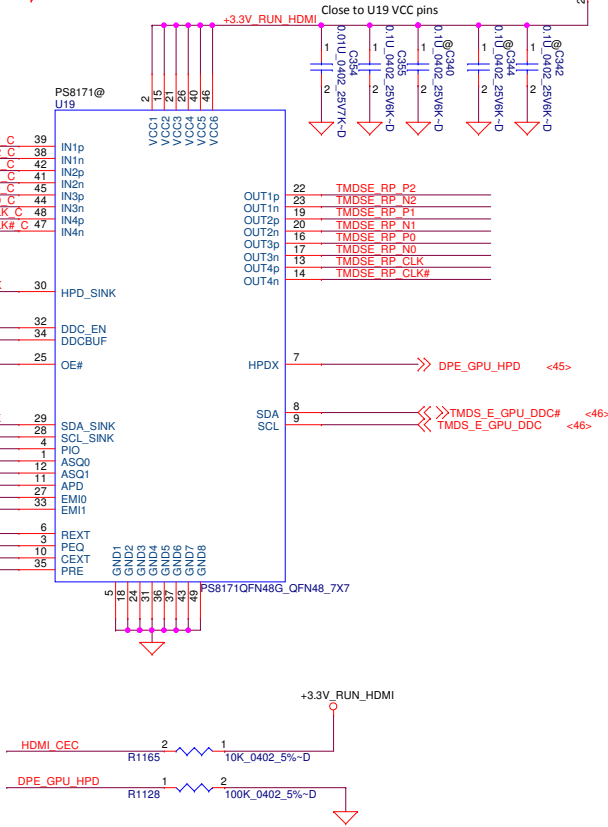
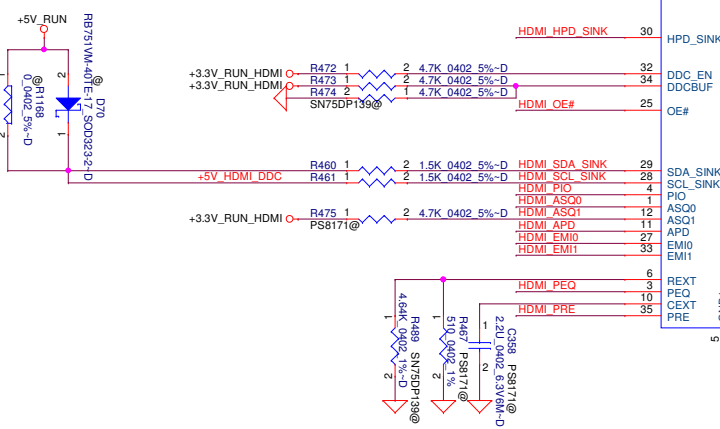
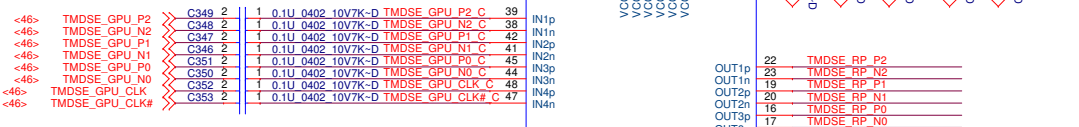
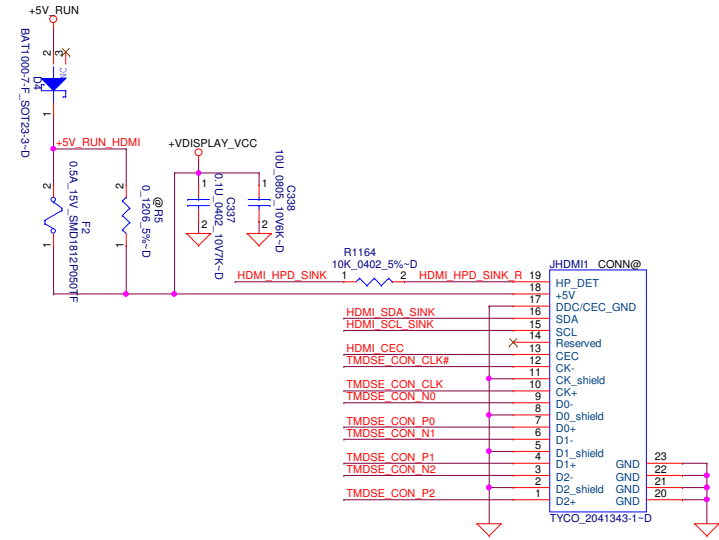
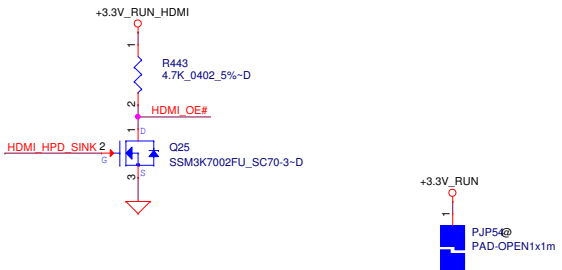
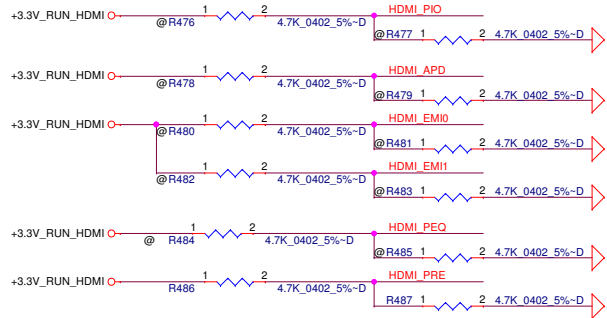


CRT_SWITCH	0	0	1	1
DGPU_SELECT#	0	1	0	1
EDID_SELECT#	0	1	0	1
	A --> Port 1	B --> Port 1	A --> Port 2	B --> Port 2

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CRT/Video switch			
Size	Document Number	Rev	
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Date:	Monday, May 28, 2012	Sheet	25 of 71

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PIN	SIGNAL	CONNECTION	SIGNAL	CONNECTION
1	ASQ0	NC	GND	Stuff R488
3	PEQ		SRC	
4	PIO		I2C_EN	Stuff R476
6	REXT	Stuff R467	VSadj	Stuff R489
10	CEXT	Stuff C358	NC	NC
11	APD	Stuff R478	VCC	Stuff R490
12	ASQ1	Stuff R475	GND	Stuff R493
27	EMI0		GND	Stuff R494
33	EMI1		VCC	Stuff R495
34	DDCBUF		HPDINV	Stuff R474
35	PRE		OVS	

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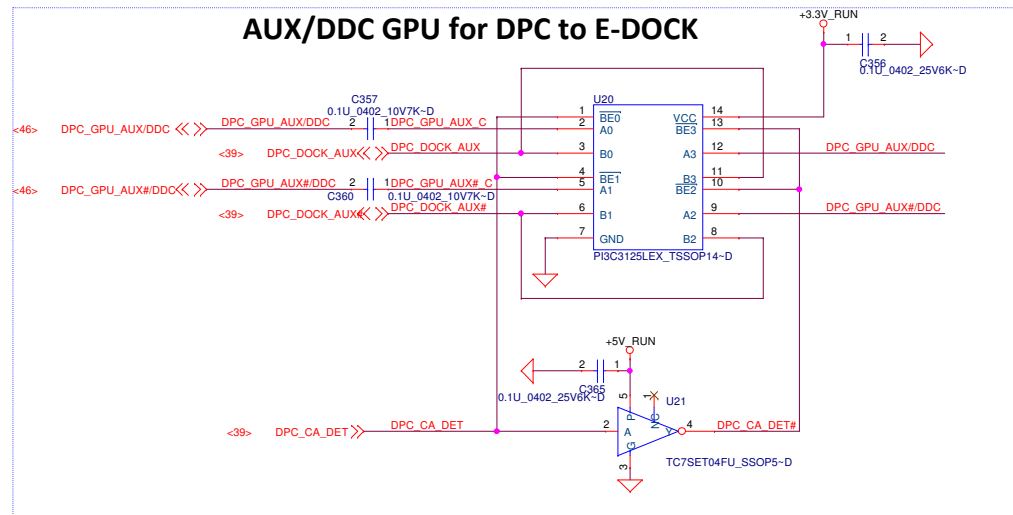
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HDMI port

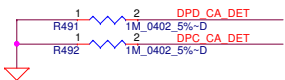
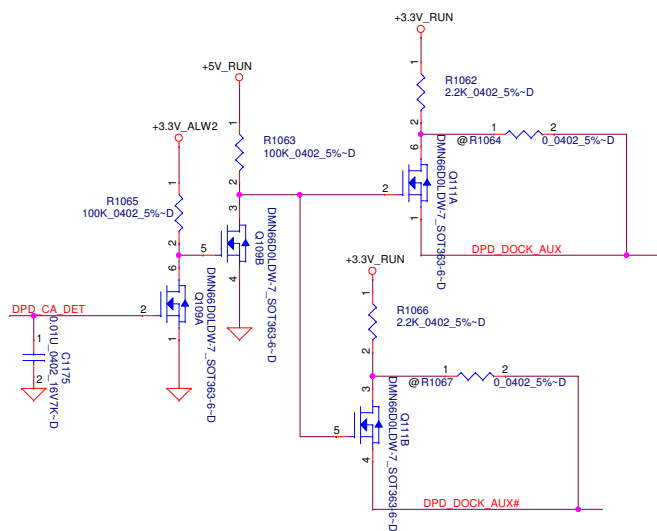
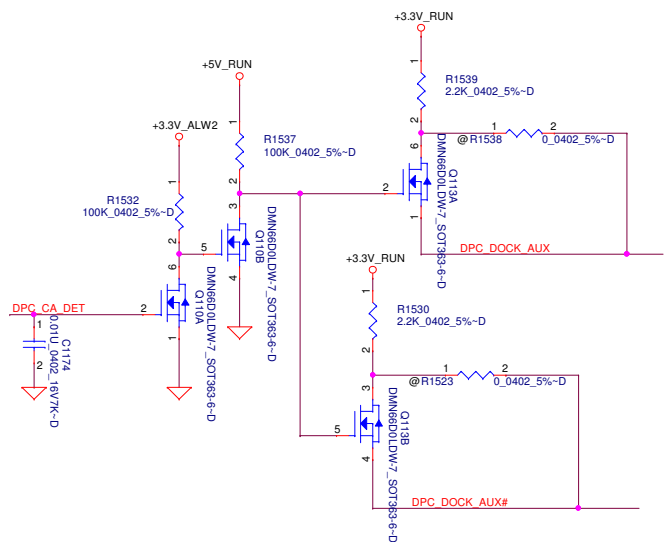
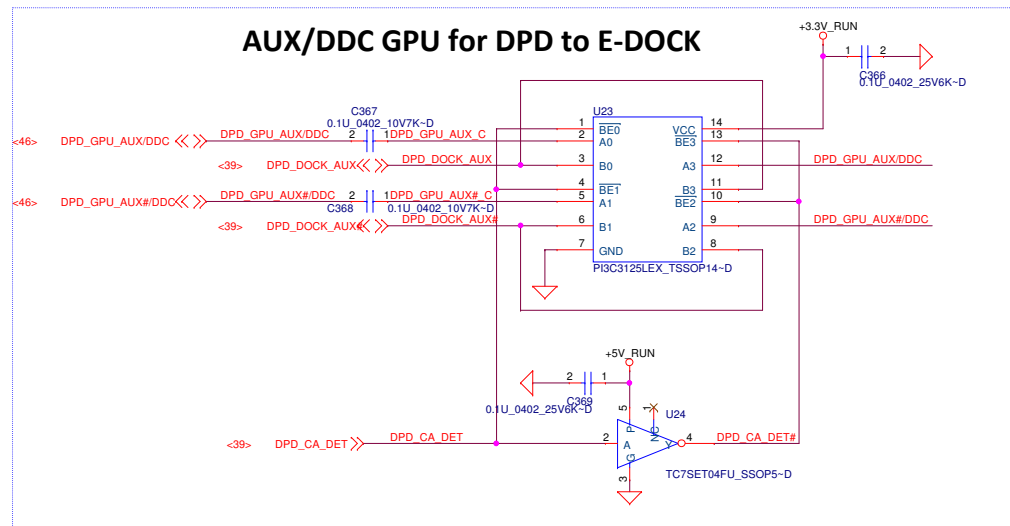
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AUX/DDC GPU for DPC to E-DOCK



AUX/DDC GPU for DPD to E-DOCK



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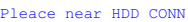
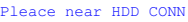
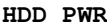


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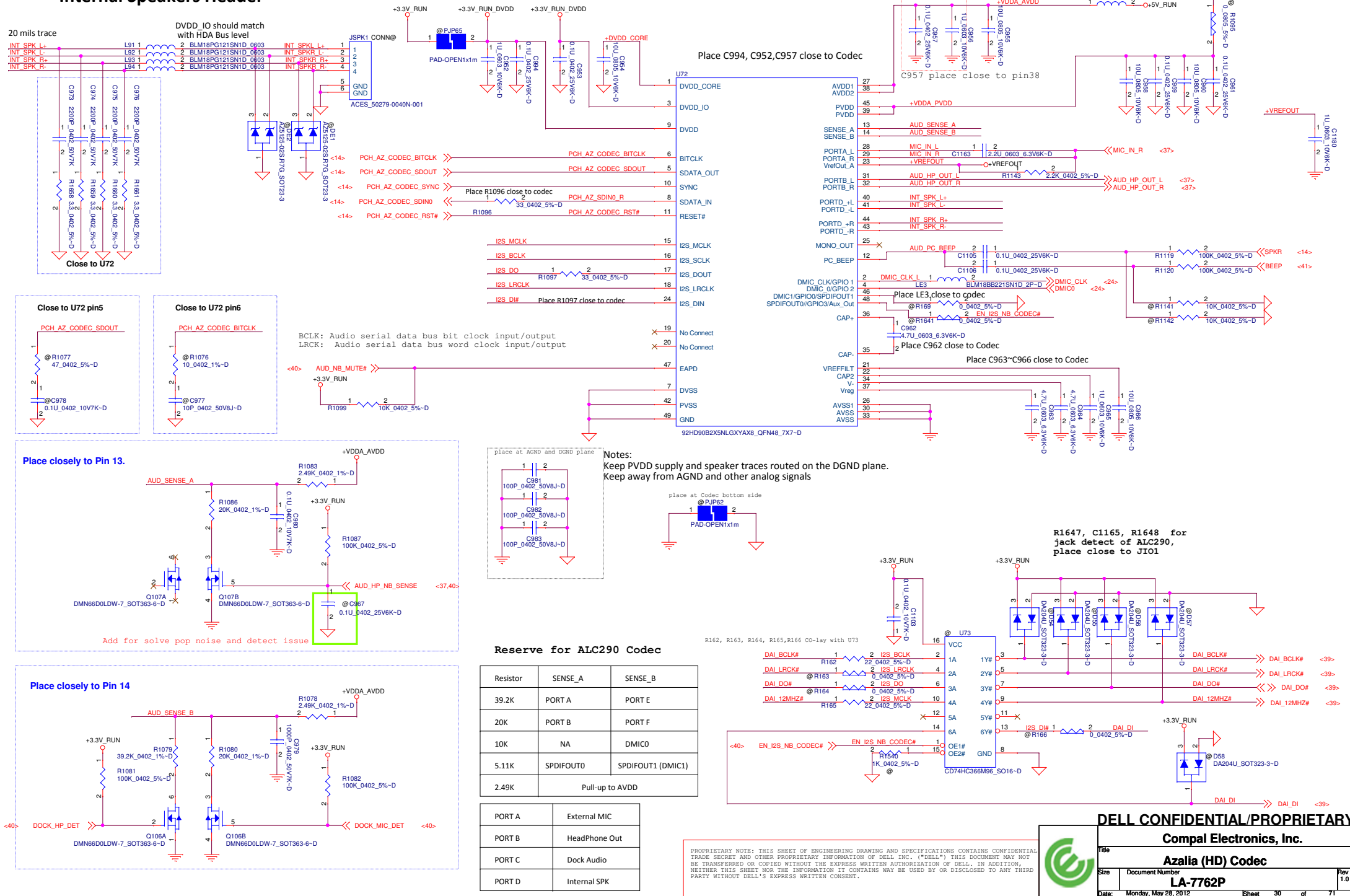
Title **DP AUX SW**

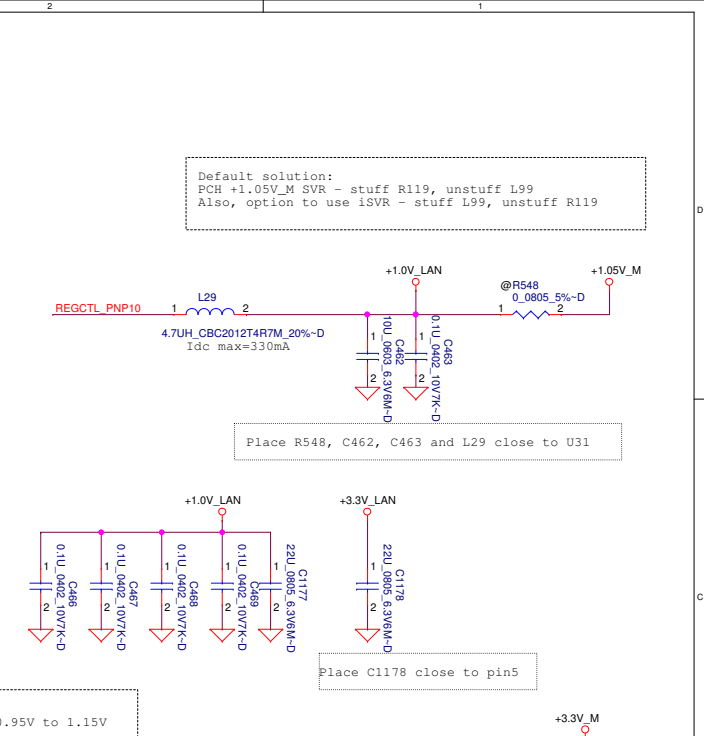
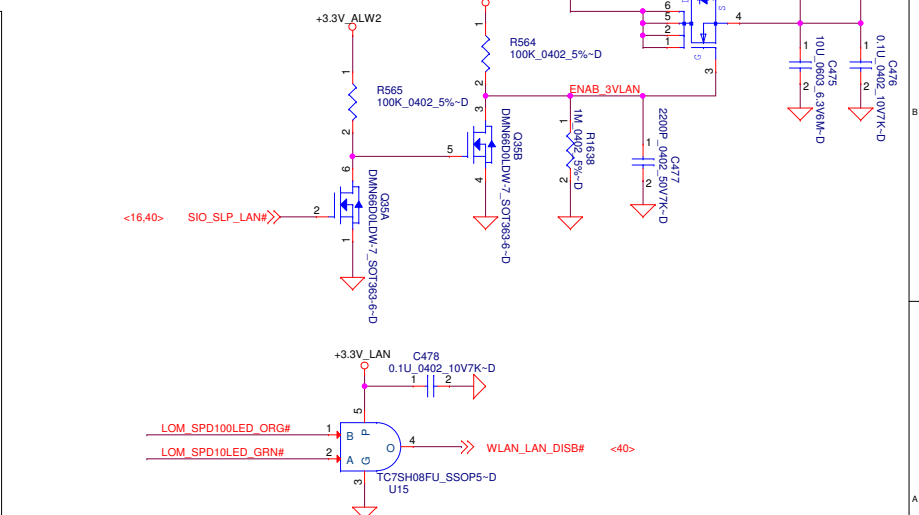
Size	Document Number	Rev
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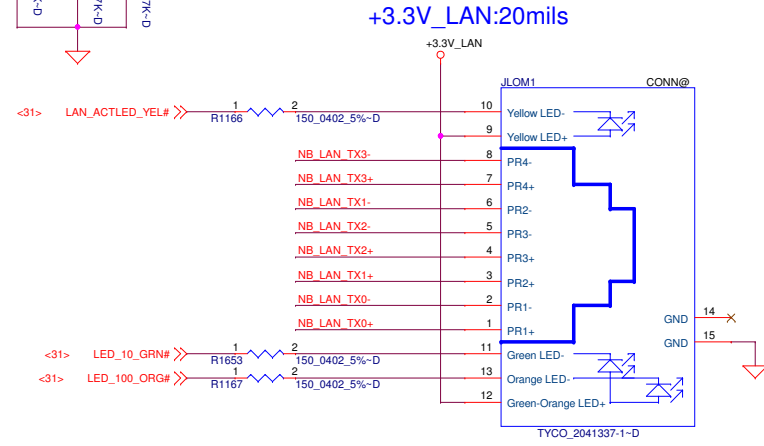
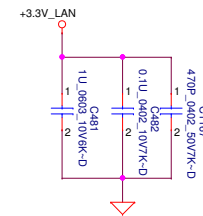
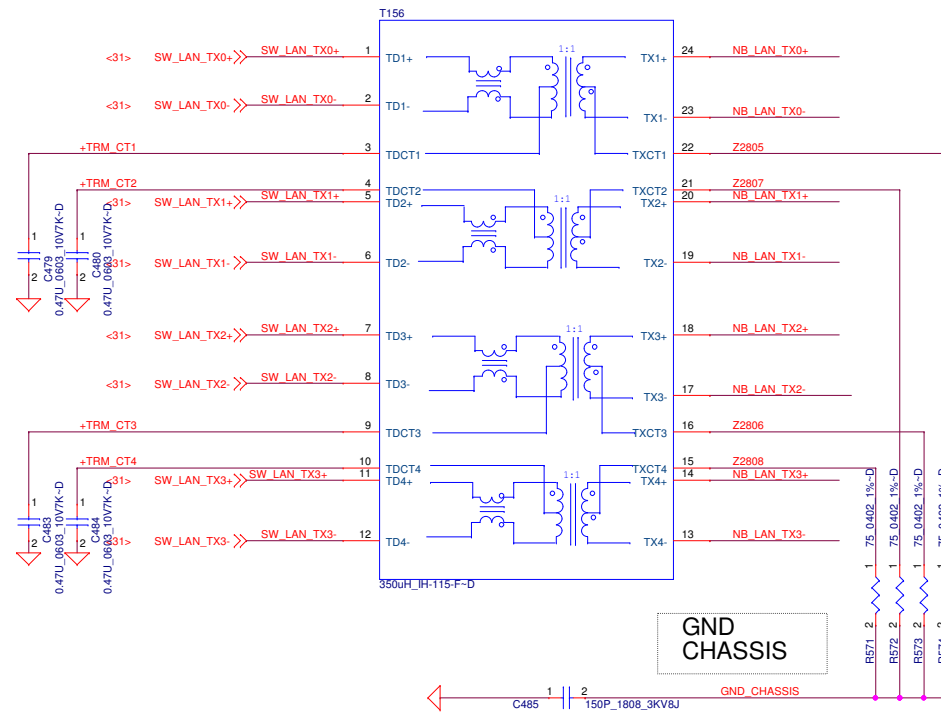


For ODD

Internal Speakers Header

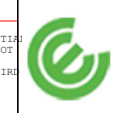


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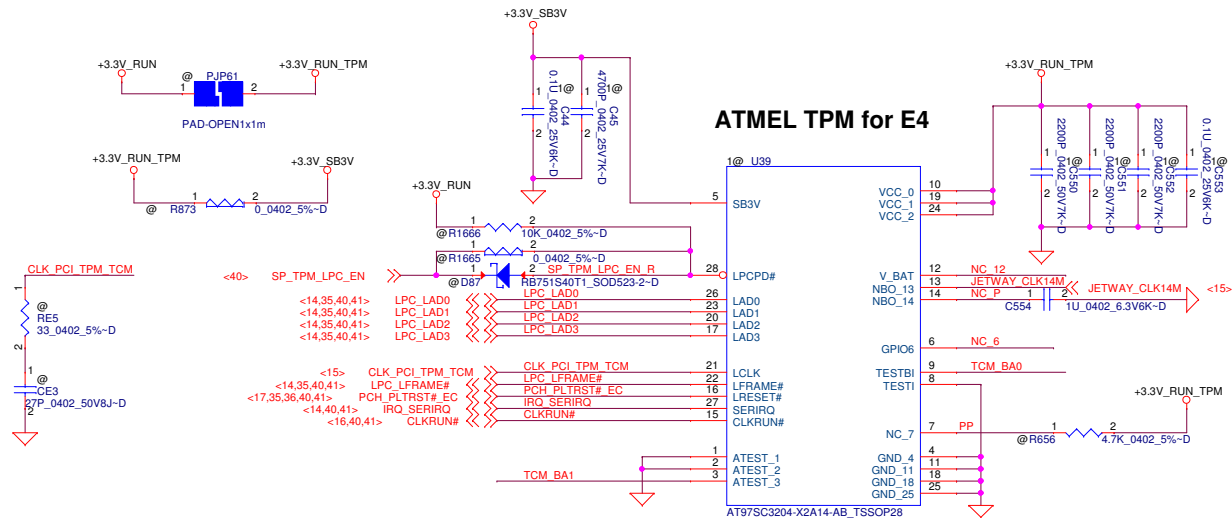


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Title			
RJ45 Conn			
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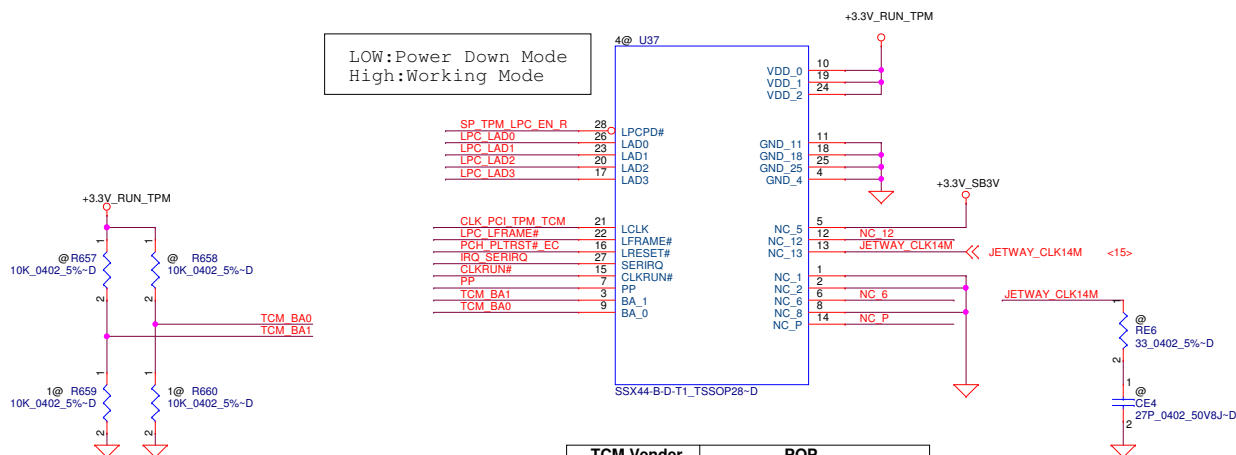


Co-lay U37 and U38

LPC layout: Place TCM first and then end LPC with TPM.

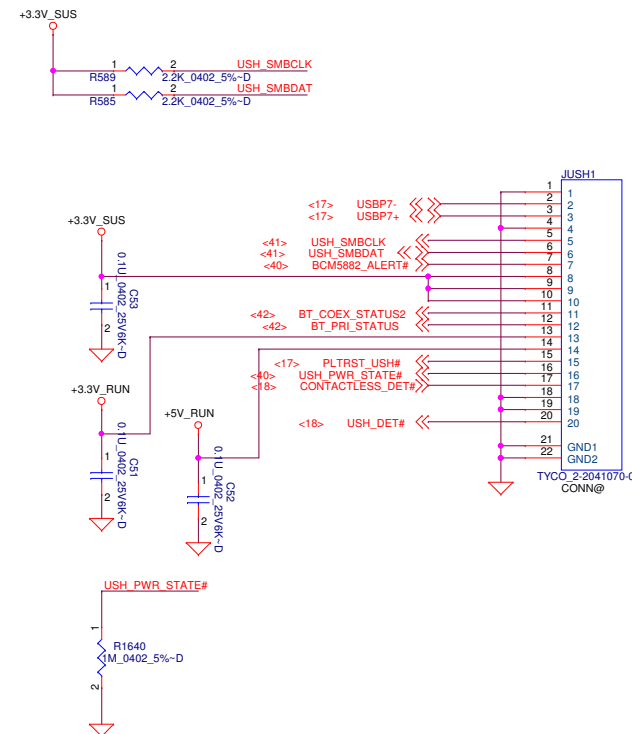
China TCM: NationZ & Jetway co-lay

LOW:Power Down Mode
High:Working Mode



TCM Vender	POP
NationZ	R660, R659, C554, C550
Jetway	C555, RH315

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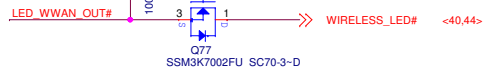


TPM and China TCM Z8H172T Option				
PART/PIN	Ref Des	TCM Enable	TPM Enable	ALL TPM/TCM Disable
TCM circuit	All 4@	POP	@	@
PCH GPIO39 ->TPM_ID1	PU RH268 PD RH271	@ POP	POP @	POP @
PCH GPIO38 ->TPM_ID0	PU RH267 PD RH270	@ POP	POP @	@ POP

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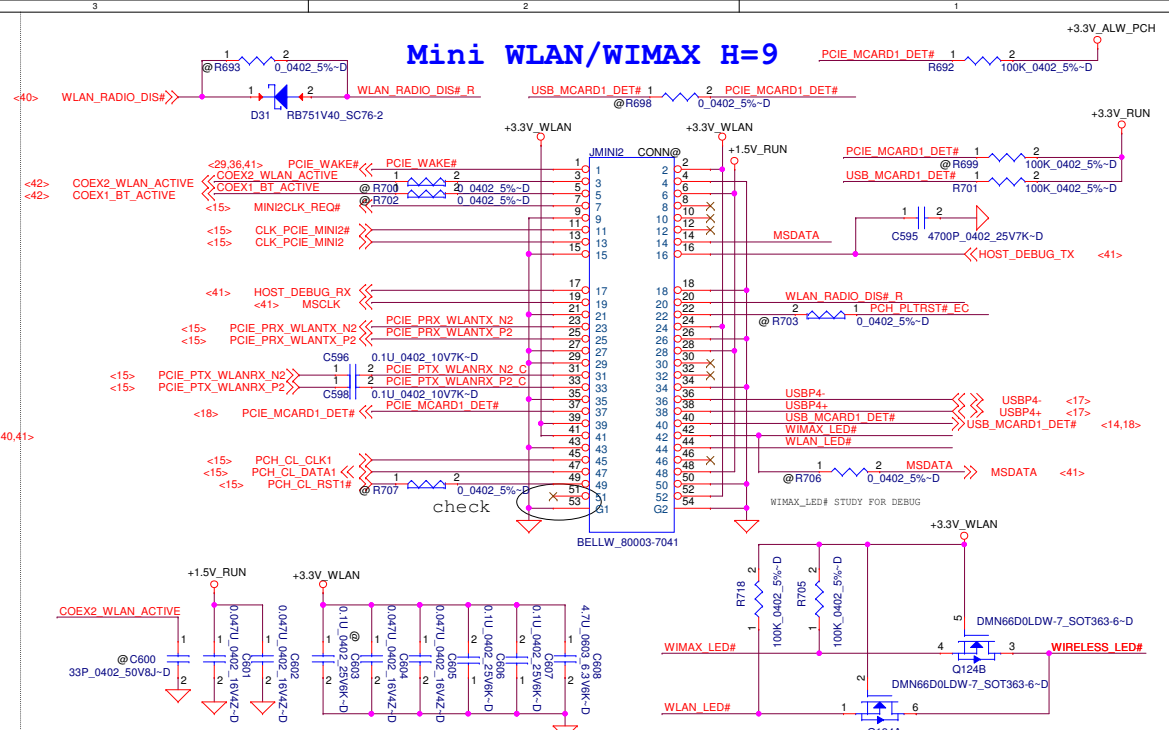
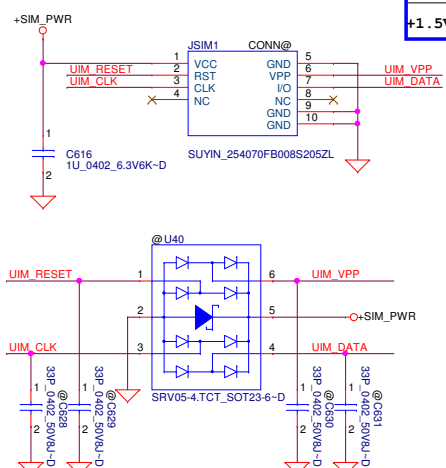
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Title			
USH conn/TPM			
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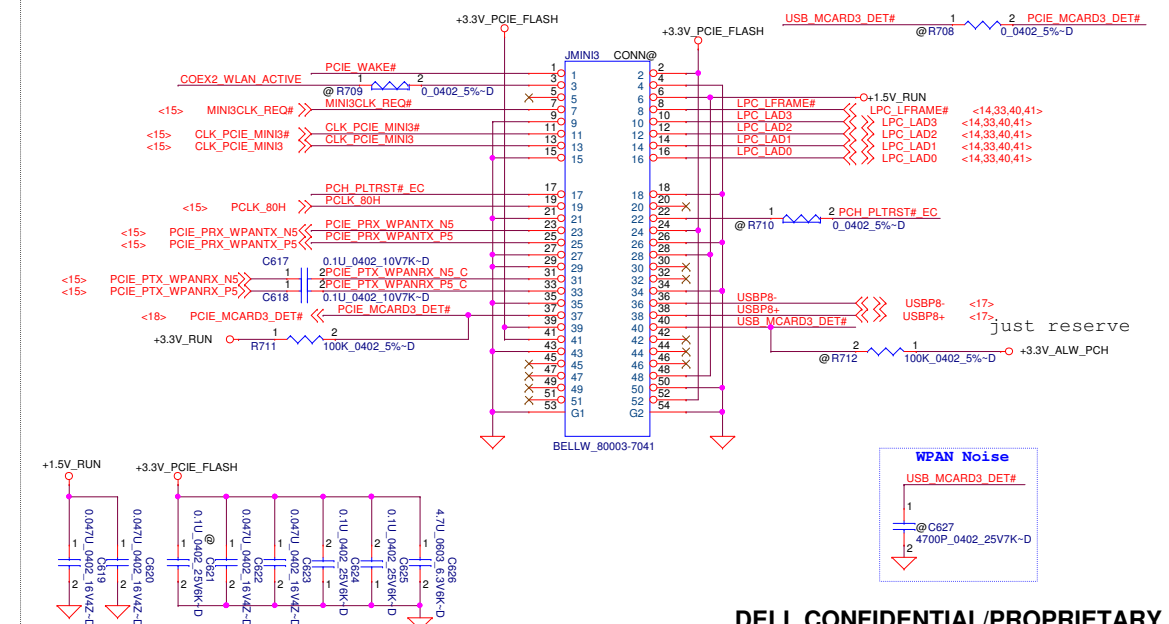


PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V	+9%	1000	750	
+3.3Vaux	+9%	330	250	250 (Wake enable) 5 (Not wake enable)
+1.5V	+5%	500	375	NA

SIM Card Push-Push



1/2 Minicard Pink Pather/60GHz Card H=9



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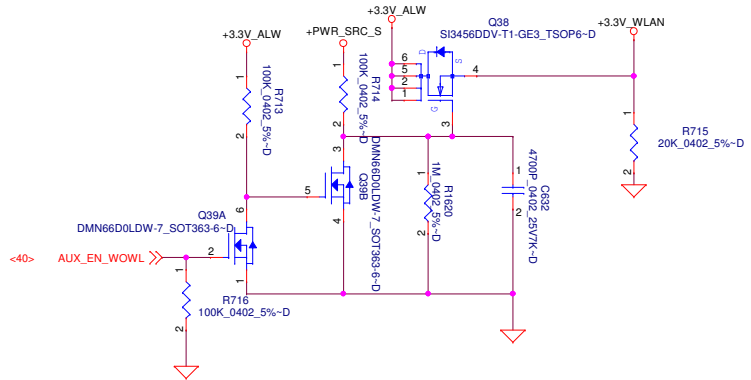
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Mini Card

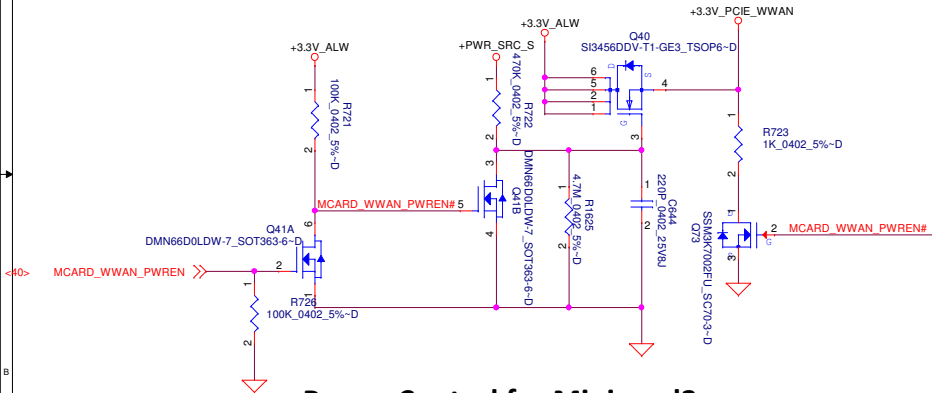
LA-7762P

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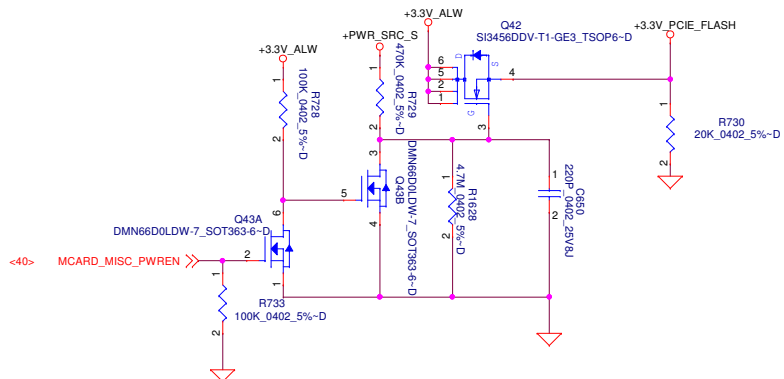
Power Control for Mini card1



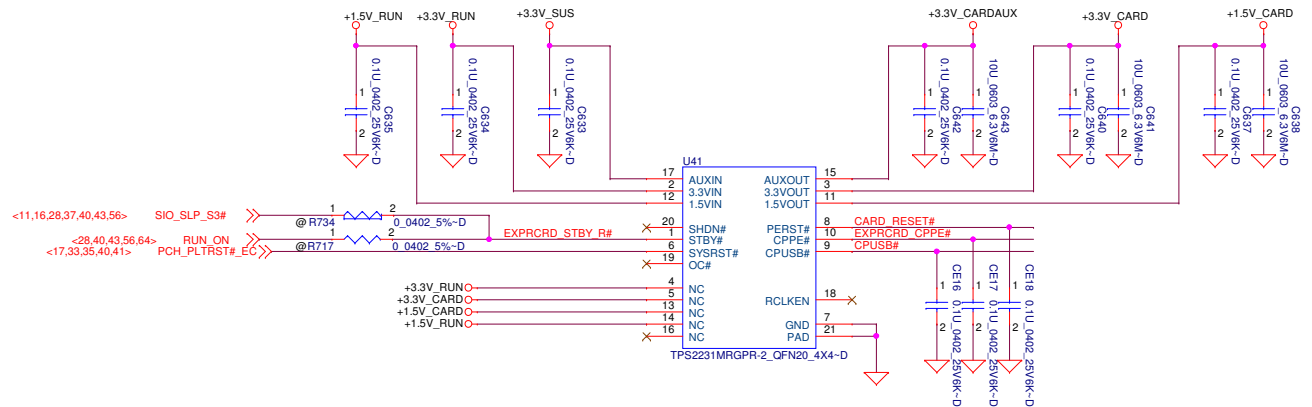
Power Control for Mini card2



Power Control for Mini card3

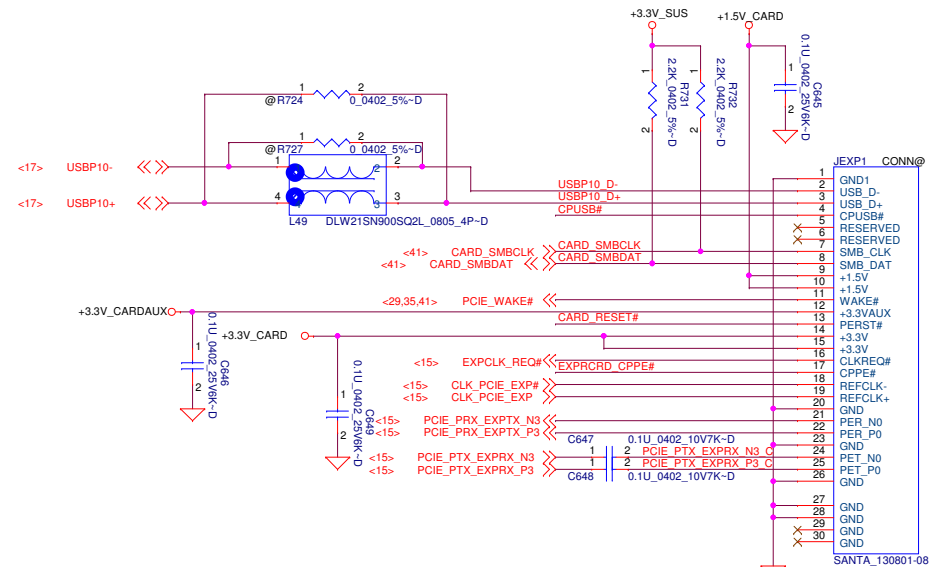


Express Card PWR S/W



Note: Add connection on pin4, pin5, pin 1 and pin14 to support GMT 2nd source part

Express Card Conn.



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PCIE-SATA SW / PCIE PWR

LA-7762P

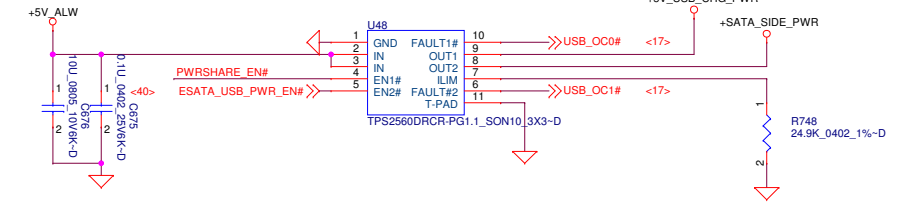
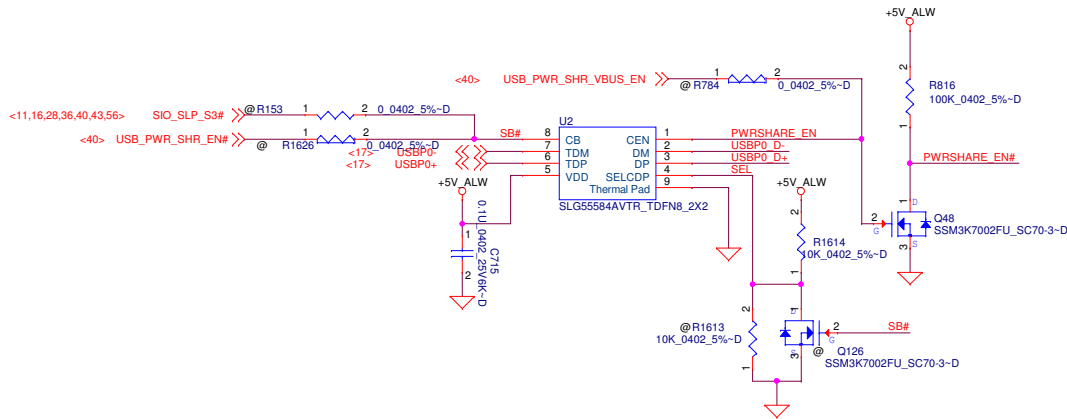
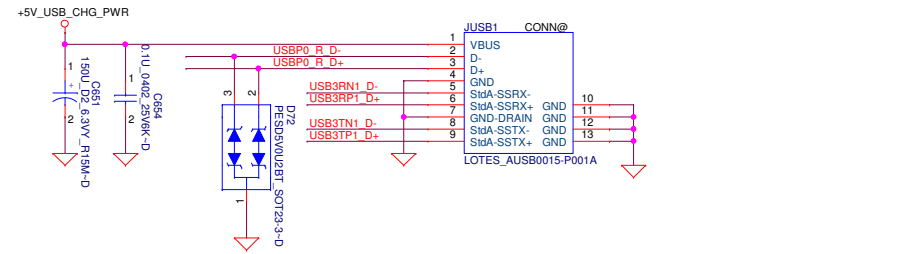
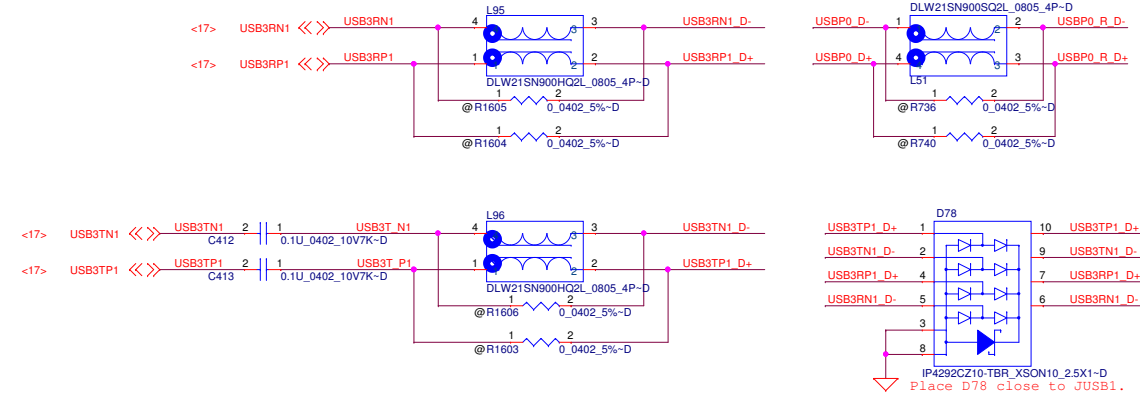
LA-7
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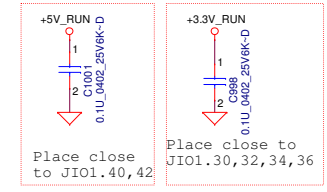
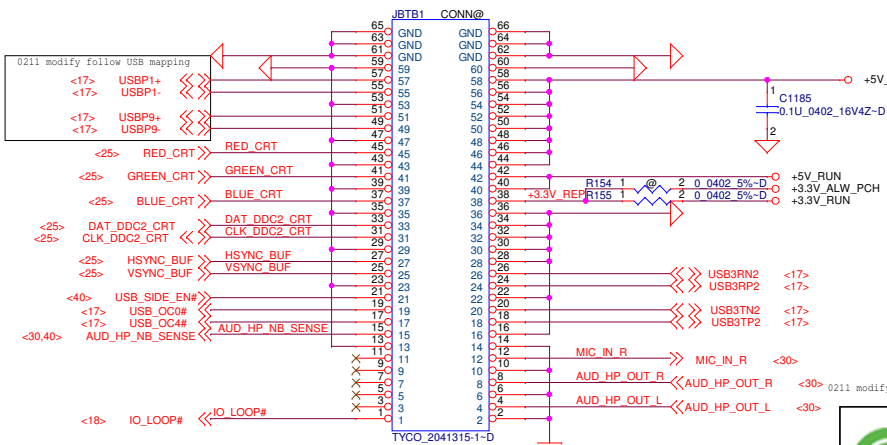
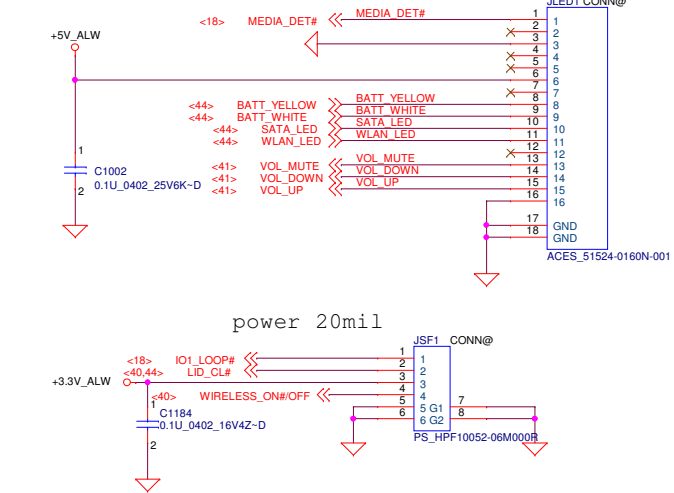
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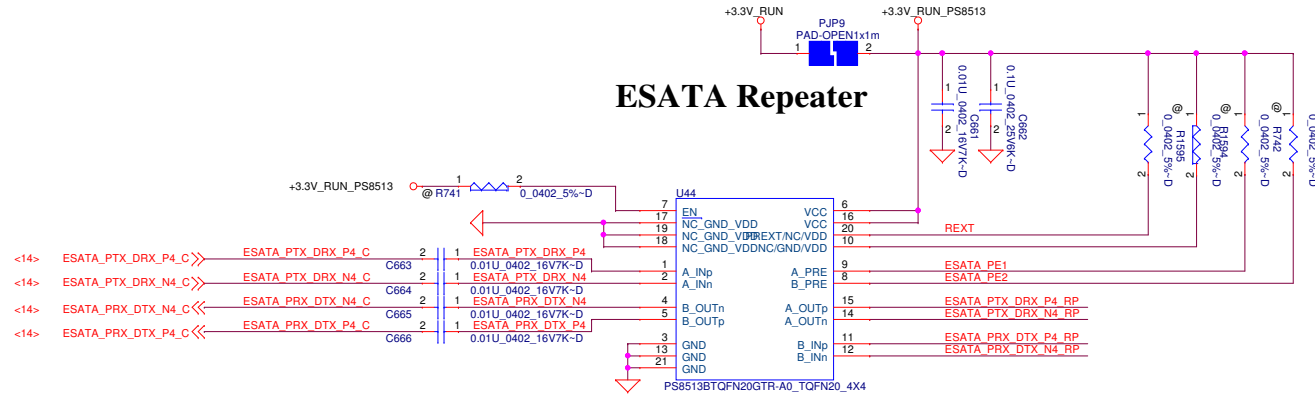
MEDIA BOARD USBx2 /USB3.0x1 / CRT/ AUDIO JACK IO BOARD

Default on,
WIRELESS_ON/OFF#:
LOW: ON
HIGH: OFF

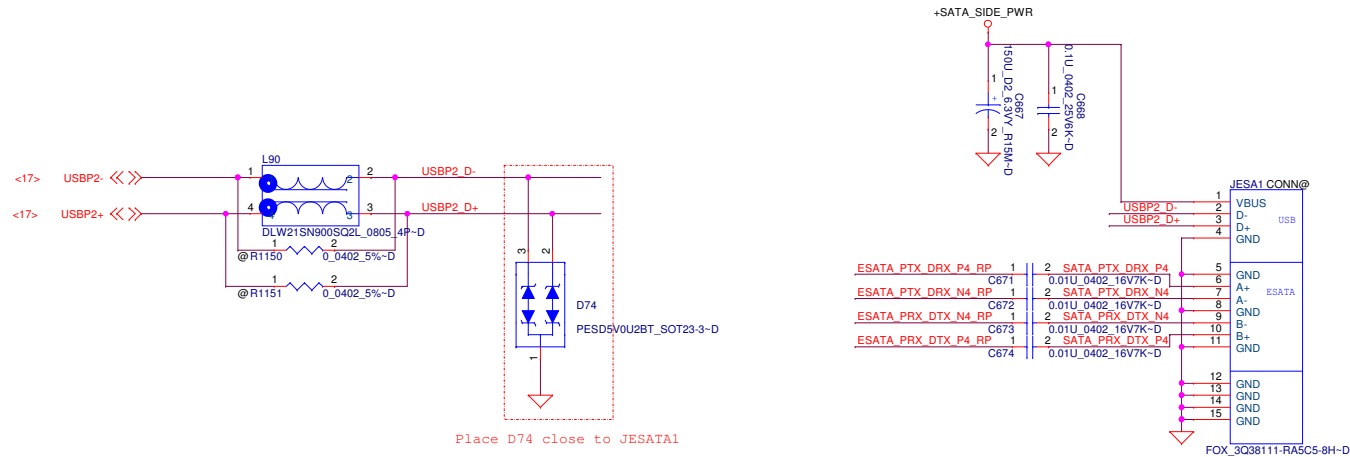


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Title	IO BOARD/ USB3.0		
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ESATA Repeater



Note: +ESATA_DEW1, +ESATA_DEW2, +ESATA_EQ1, +ESATA_EQ2 need to route 10 mils and R1584~R1587 need to change to 10k and no stuff R1584, R1585 to support TI SN75LVCP601



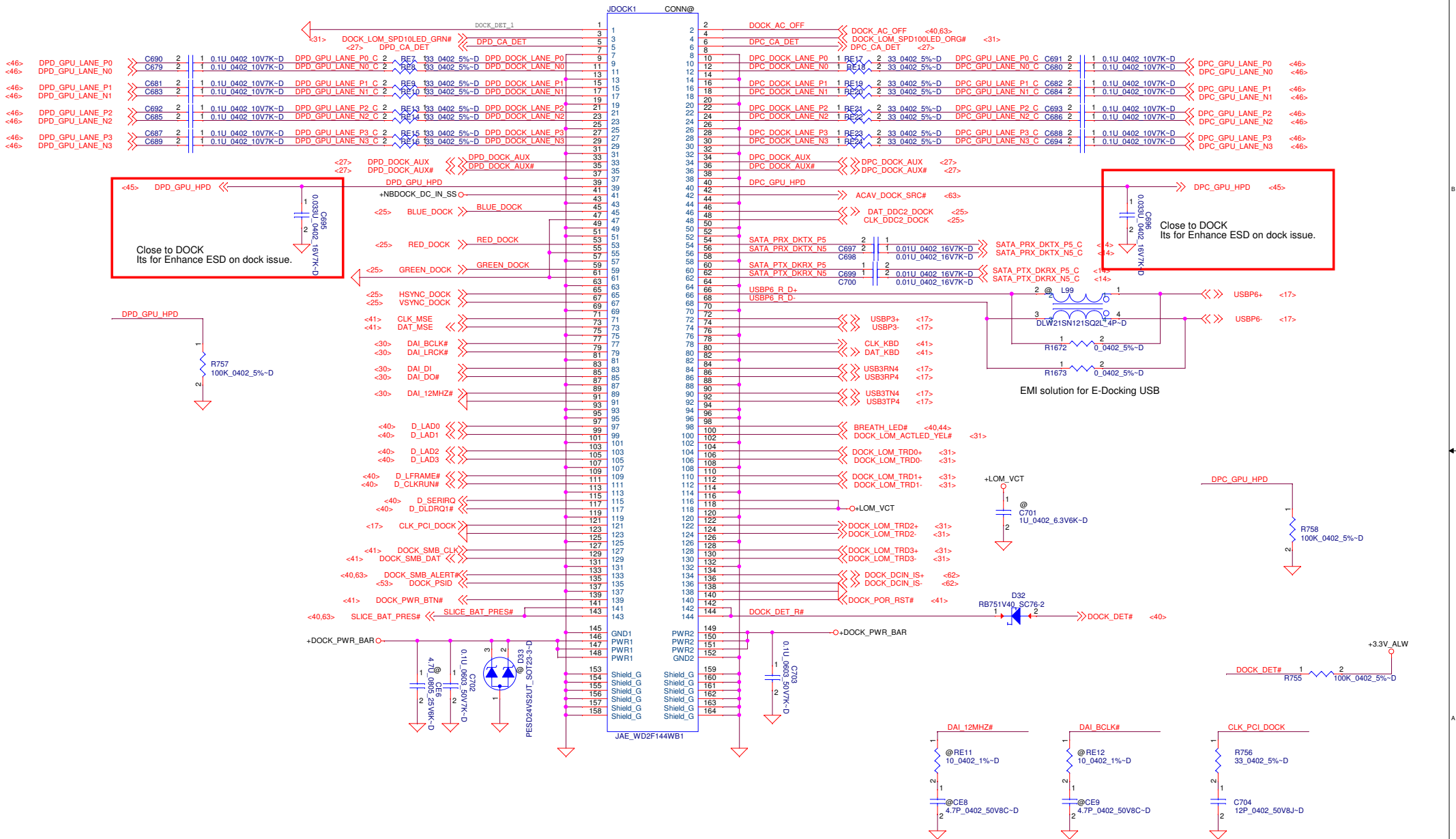
Place D74 close to JESATA1

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Title			
USB/ESATA/IO/MDC			
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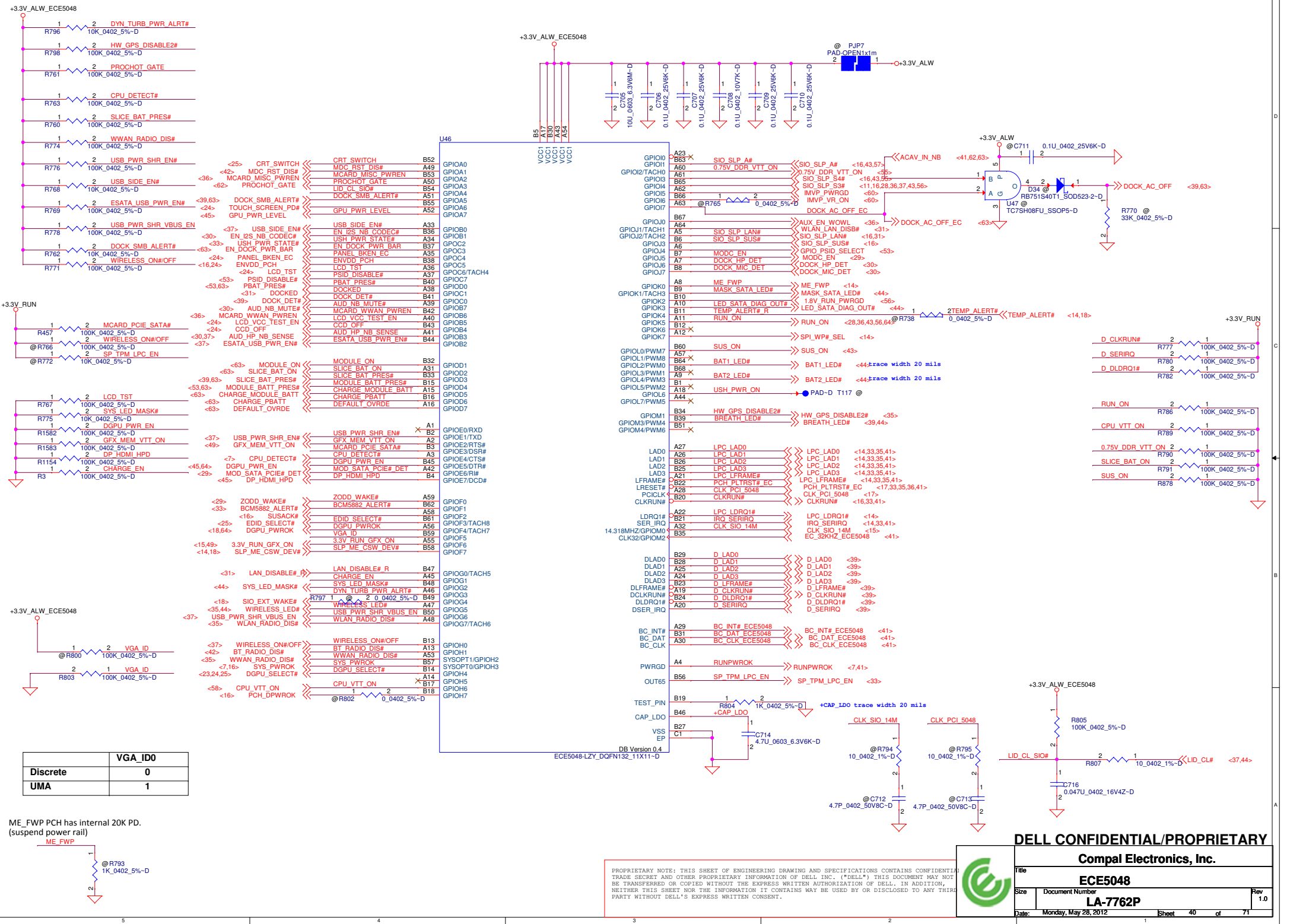
Compal Electronics, Inc.

DOCKING CONN

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Title		Rev
Size	Document Number	1.0



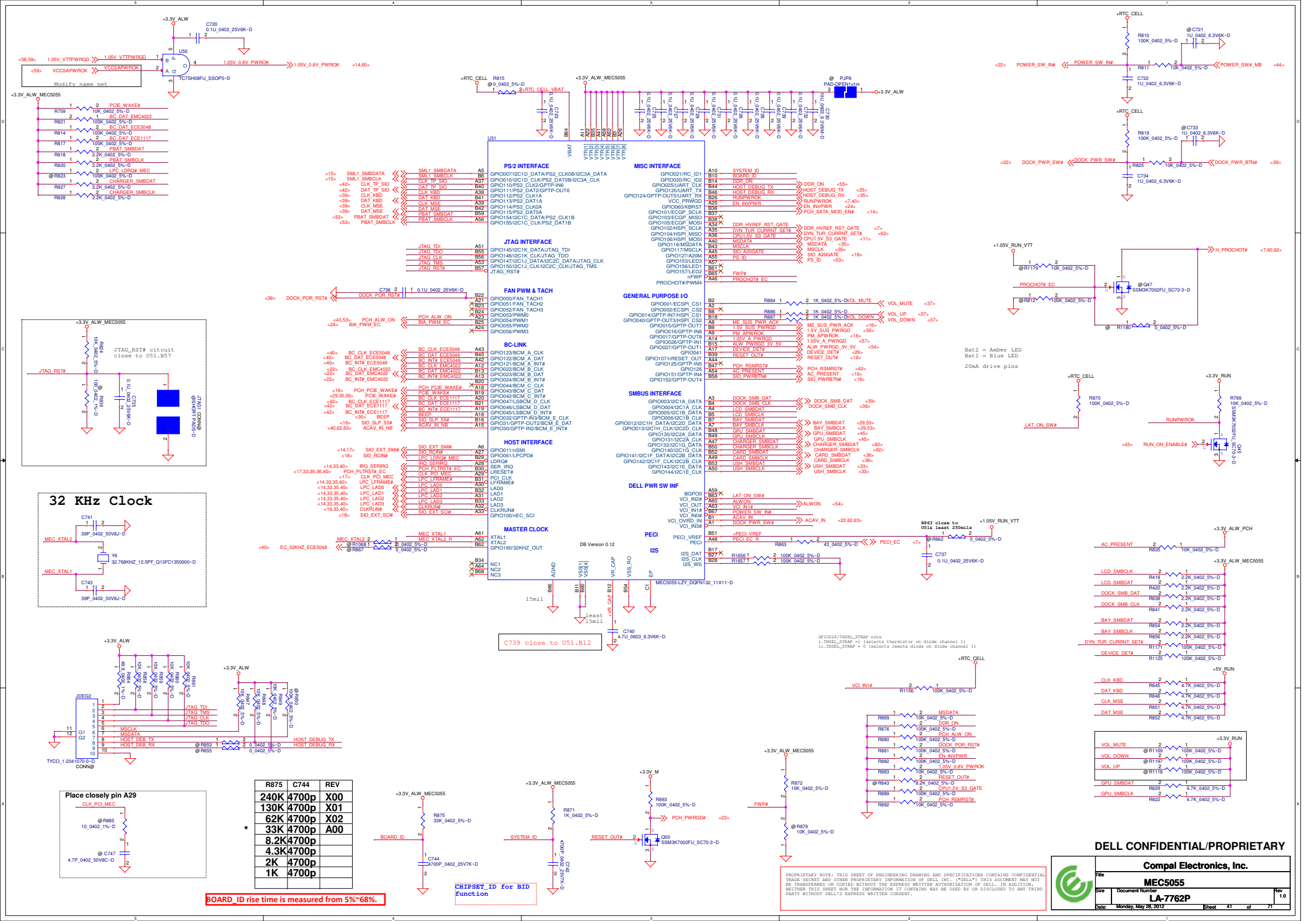
	VGA_ID0
Discrete	0
UMA	1

ME_FWP PCH has internal 20K PD.
(suspend power rail)

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Compal Electronics, Inc.			
ECE5048			
LA-7762P			
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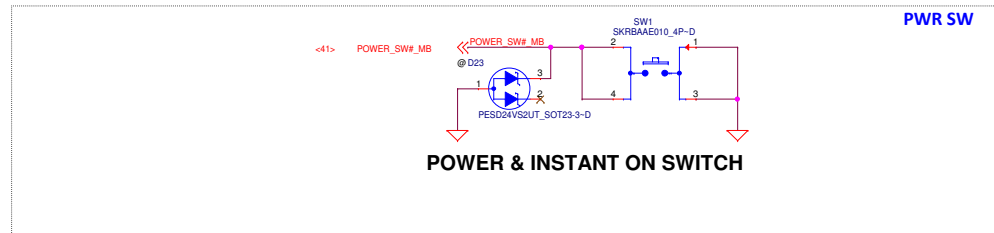
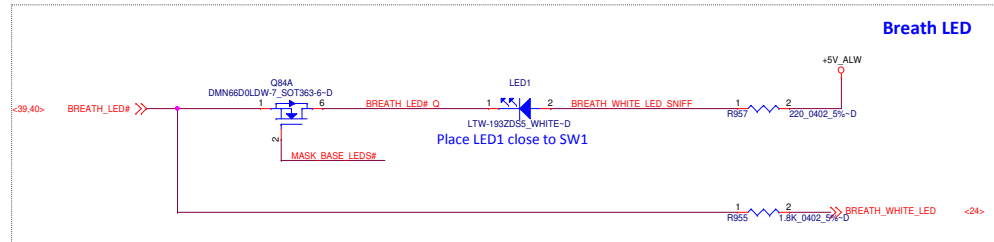
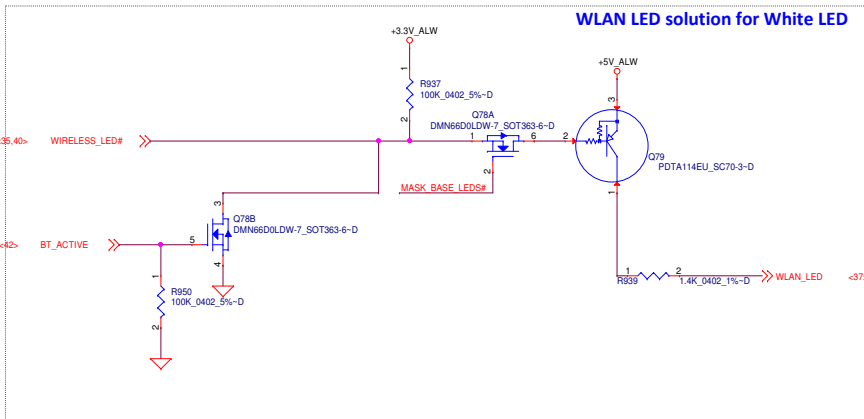
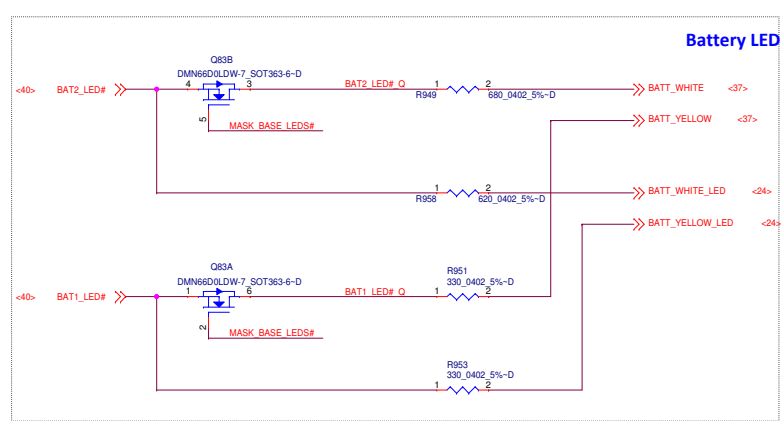
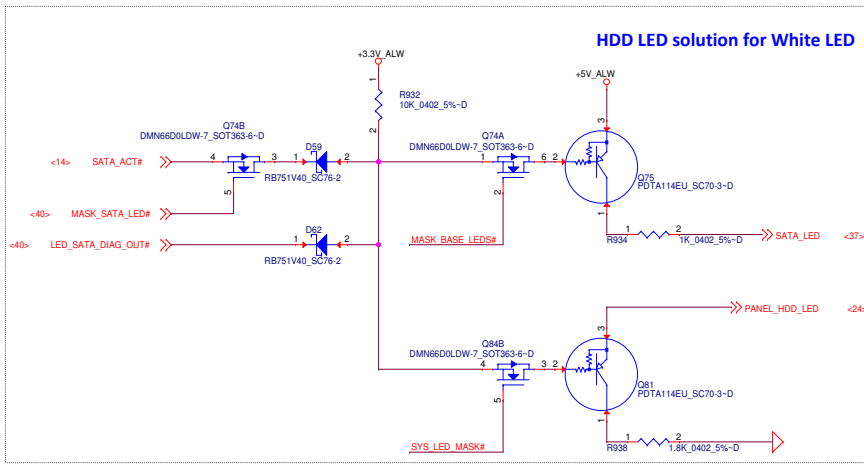
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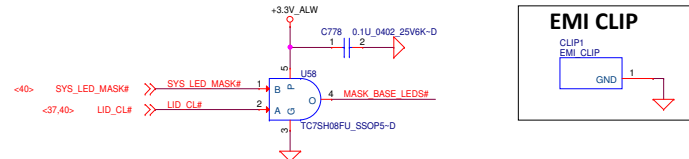
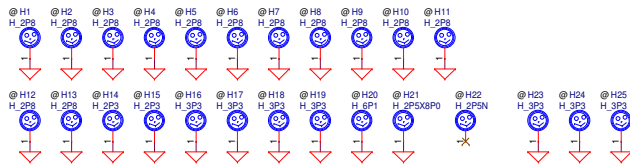
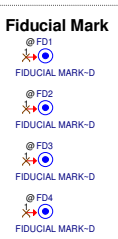
The schematic diagram illustrates the SUS control circuit. It features a +3.3V ALW2 supply connected to a network of resistors (R911, R915, R1607, R1608, R1618) and MOSFETs (Q53A, Q53B). The circuit includes a pull-up resistor (R1618) and a capacitor (C767) connected to the SUS ENABLE signal. The output of the circuit is labeled SUS ON 3.3V#.

[illegible]

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LED Circuit Control Table		
	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1



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PWR SW/LED/PAD/ME

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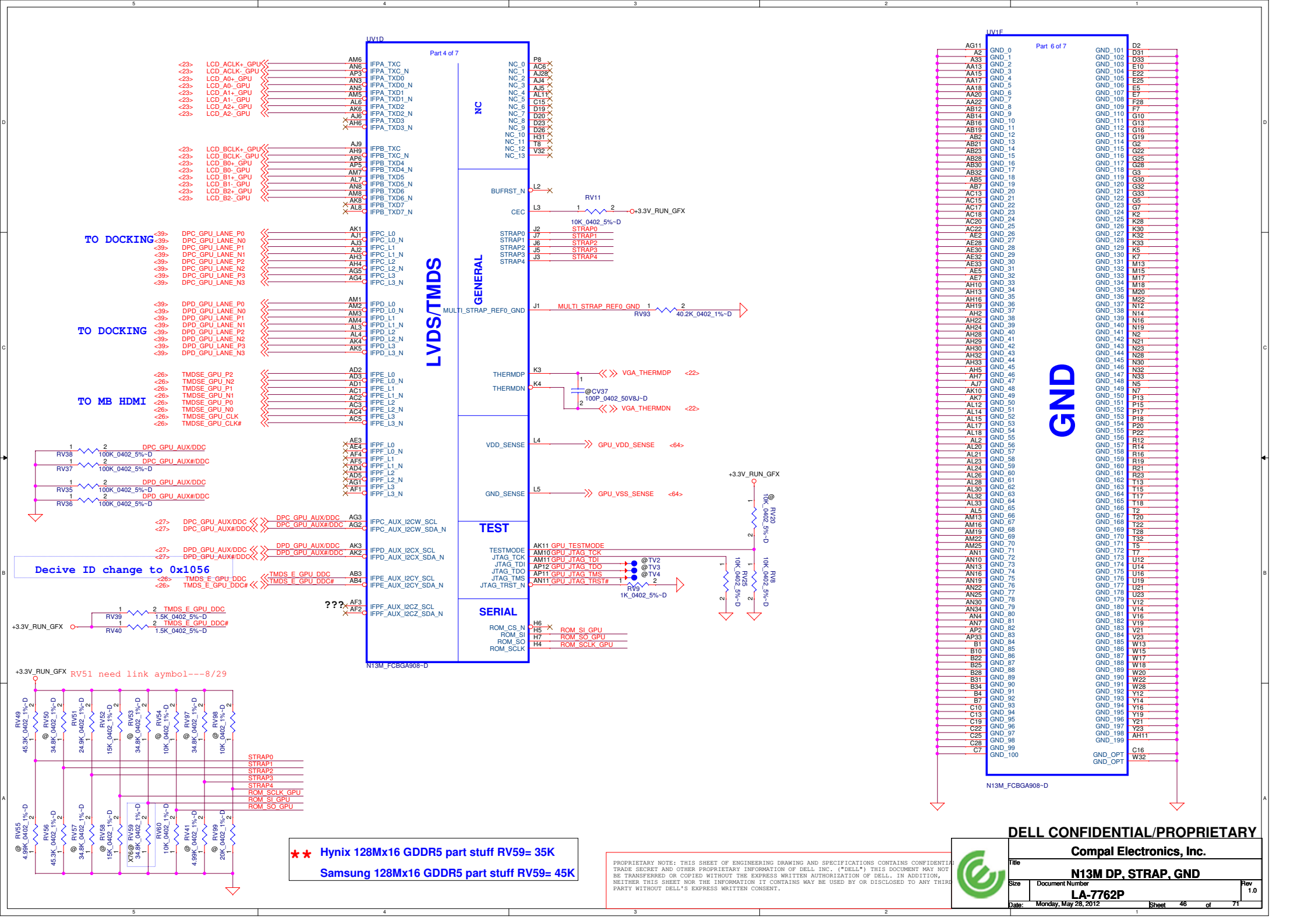
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1.0

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close to the GPU

Close to Pin

Part 5 of 7

POWER

PLACE UNDER BGA

PLACE NEAR GPU

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Compal Electronics, Inc.

N13M Power

LA-7762P

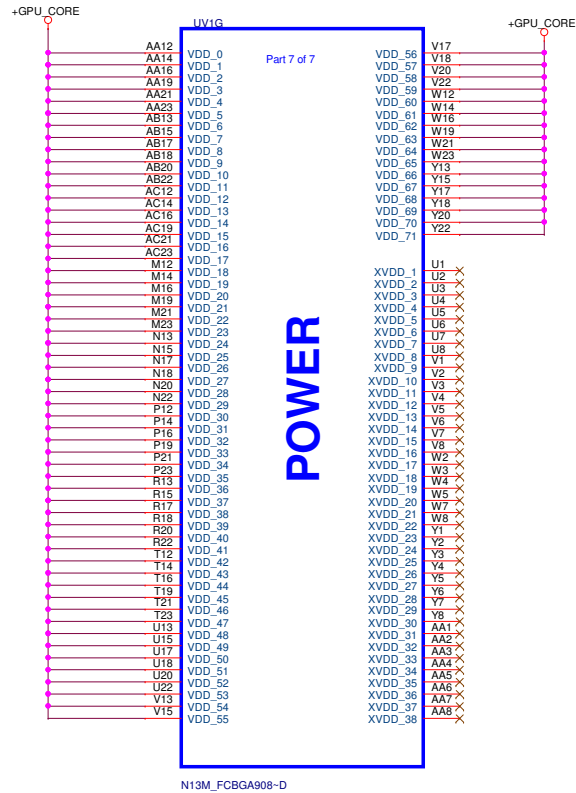
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Rev 1.0

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Caps on Power Side



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Title			
N13M Power GFX Core			
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FBA_D[0..31] <>> FBA_D[0..31] <51>
FBA_D[32..63] <>> FBA_D[32..63] <52>
FBA_CMD[0..31] <>> FBA_CMD[0..31] <51,52>
FBA_DB[4..7] <>> FBA_DB[4..7] <52>
FBA_DB[0..3] <>> FBA_DB[0..3] <51>
FBA_EDC[4..7] <>> FBA_EDC[4..7] <52>
FBA_EDC[0..3] <>> FBA_EDC[0..3] <51>

GDDR5 CMD Mapping Table

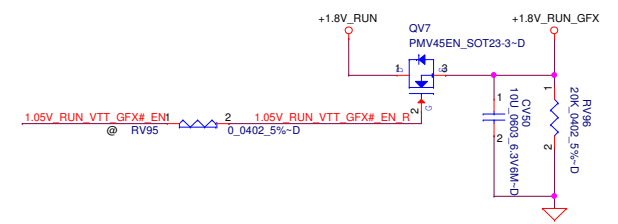
<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD6	CS#
CMD24	CMD14	AB1#
CMD8	CMD26	A0 A10
CMD10	CMD26	A1 A9
CMD11	CMD18	A2 BA0
CMD2	CMD17	A3 BA3
CMD1	CMD19	A4 BA2
CMD3	CMD20	A5 BA1
CMD7	CMD23	A6 A11
CMD6	CMD22	A7 A8
CMD9	CMD25	A12 FRU
CMD14	CMD25	CKE#
CMD13	CMD29	RESET#

MEMORY INTERFACE

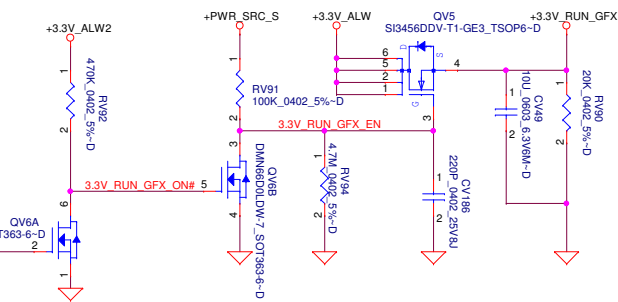
FBA_D0 L28	FBA_D00	U30	FBA_CMD0
FBA_D1 M29	FBA_D01	T31	FBA_CMD1
FBA_D2 L29	FBA_D02	U29	FBA_CMD2
FBA_D3 M28	FBA_D03	R34	FBA_CMD3
FBA_D4 N31	FBA_D04	R33	FBA_CMD4
FBA_D5 P29	FBA_D05	U32	FBA_CMD5
FBA_D6 R29	FBA_D06	U33	FBA_CMD6
FBA_D7 P28	FBA_D07	U28	FBA_CMD7
FBA_D8 J28	FBA_D08	V28	FBA_CMD8
FBA_D9 H29	FBA_D09	V29	FBA_CMD9
FBA_D10 J29	FBA_D10	V30	FBA_CMD10
FBA_D11 H28	FBA_D11	U34	FBA_CMD11
FBA_D12 G29	FBA_D12	U31	FBA_CMD12
FBA_D13 E31	FBA_D13	V34	FBA_CMD13
FBA_D14 J32	FBA_D14	V33	FBA_CMD14
FBA_D15 F30	FBA_D15	V32	FBA_CMD15
FBA_D16 C34	FBA_D16	AA31	FBA_CMD16
FBA_D17 D32	FBA_D17	AA29	FBA_CMD17
FBA_D18 B33	FBA_D18	AA28	FBA_CMD18
FBA_D19 C33	FBA_D19	AC34	FBA_CMD19
FBA_D20 F33	FBA_D20	AC33	FBA_CMD20
FBA_D21 F32	FBA_D21	AA32	FBA_CMD21
FBA_D22 H33	FBA_D22	AA33	FBA_CMD22
FBA_D23 H32	FBA_D23	Y28	FBA_CMD23
FBA_D24 P34	FBA_D24	Y29	FBA_CMD24
FBA_D25 P32	FBA_D25	W31	FBA_CMD25
FBA_D26 F31	FBA_D26	Y30	FBA_CMD26
FBA_D27 P33	FBA_D27	AA34	FBA_CMD27
FBA_D28 L31	FBA_D28	Y31	FBA_CMD28
FBA_D29 L34	FBA_D29	Y34	FBA_CMD29
FBA_D30 L32	FBA_D30	Y33	FBA_CMD30
FBA_D31 L33	FBA_D31	V31	FBA_CMD31
FBA_D32 AG28	FBA_D32	FBA_CMD31	
FBA_D33 AF29	FBA_D33		
FBA_D34 AG28	FBA_D34		
FBA_D35 AF28	FBA_D35		
FBA_D36 AD30	FBA_D36		
FBA_D37 AD29	FBA_D37		
FBA_D38 AC29	FBA_D38		
FBA_D39 AD28	FBA_D39		
FBA_D40 AJ29	FBA_D40		
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FBA_D42 AJ30	FBA_D42		
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FBA_D45 AM31	FBA_D45		
FBA_D46 AN29	FBA_D46		
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FBA_D48 AN31	FBA_D48		
FBA_D49 AN32	FBA_D49		
FBA_D50 AP30	FBA_D50		
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FBA_D58 AC30	FBA_D58		
FBA_D59 AD31	FBA_D59		
FBA_D60 AF31	FBA_D60		
FBA_D61 AG34	FBA_D61		
FBA_D62 AG32	FBA_D62		
FBA_D63 AG33	FBA_D63		

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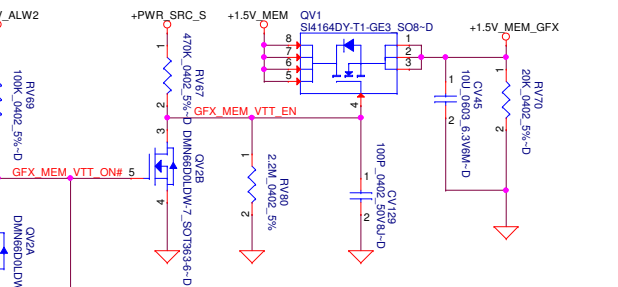
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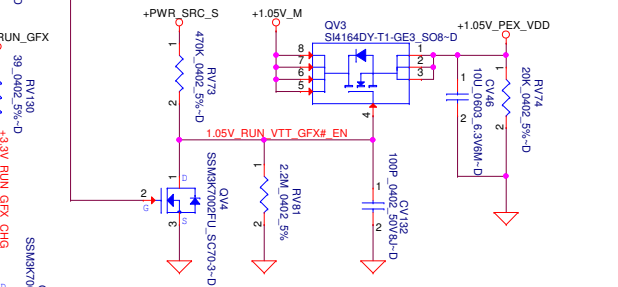
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
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+1.05V_RUN_VTT_GFX Source



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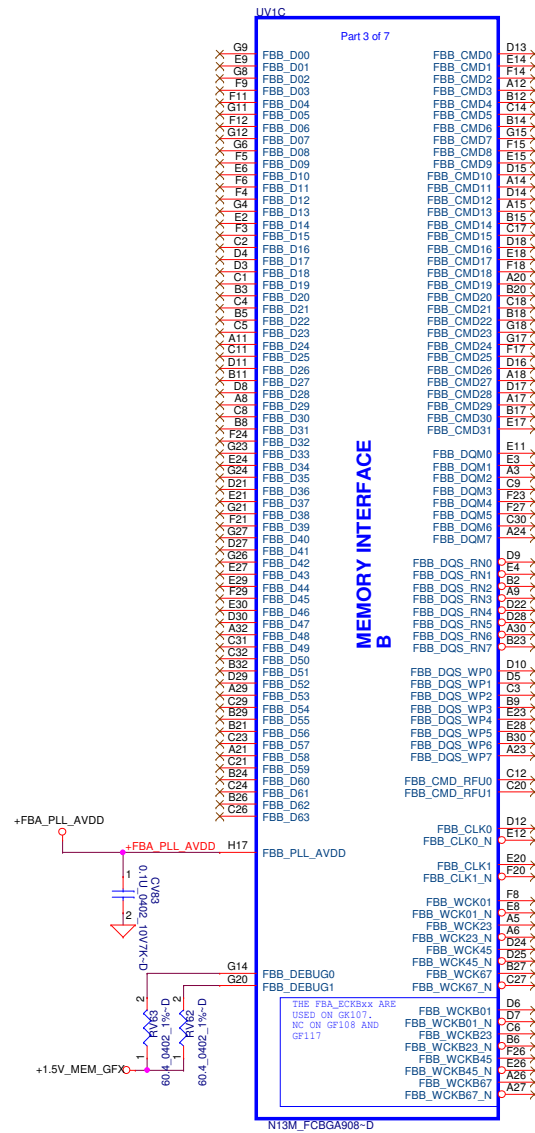


Compal Electronics, Inc.
N13M Memory
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CHANNEL-B NOT TO USE, NEED TO BE DISABLED

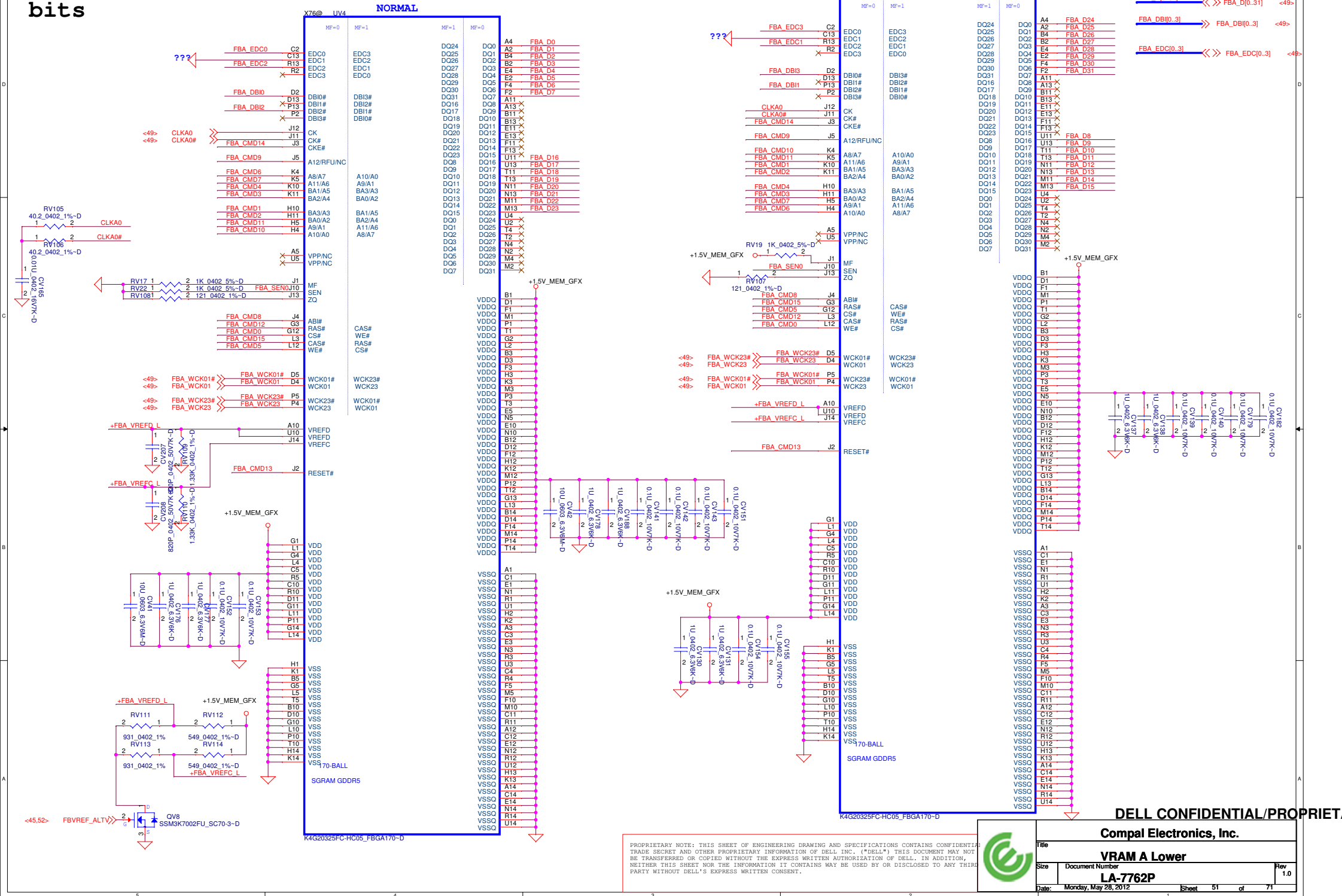


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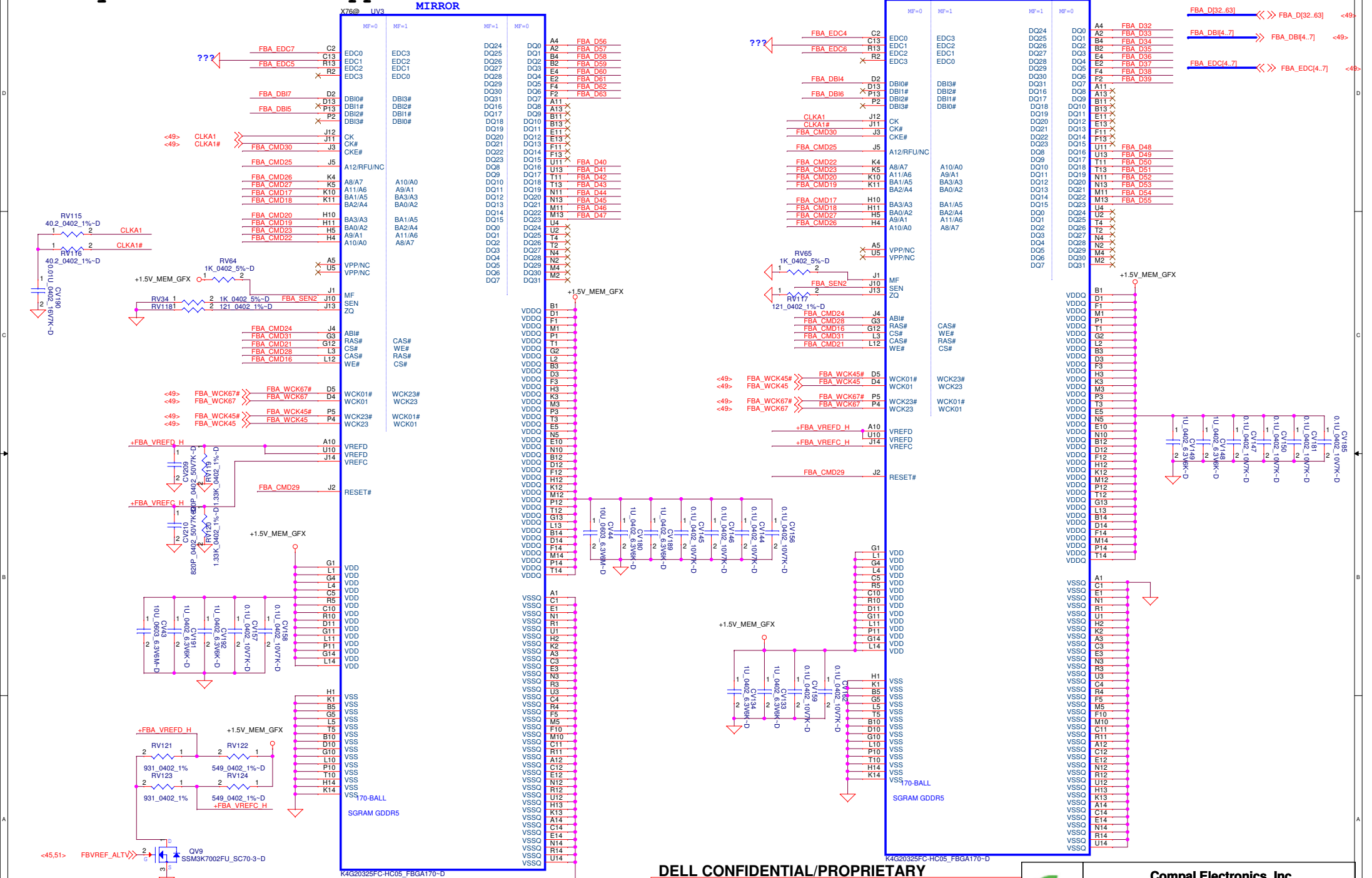
VRAM A Lower

LA-7762P

Title			
VRAM A Lower			
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Memory Partition A - Upper 32 bits



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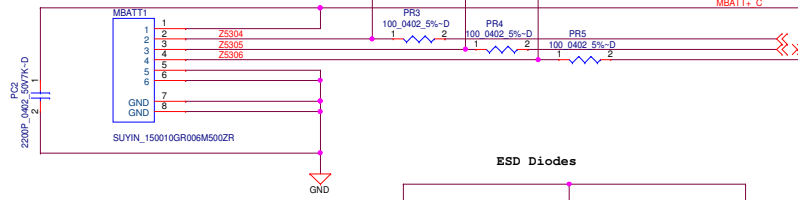
Compal Electronics, Inc.

VRAM A Upper

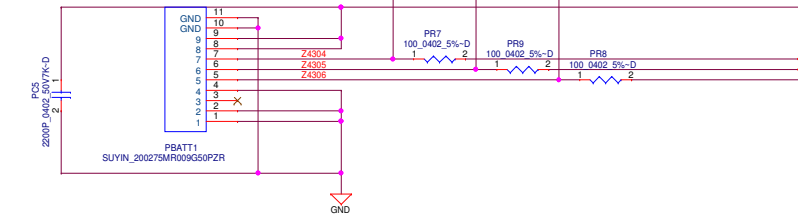
LA-7762P

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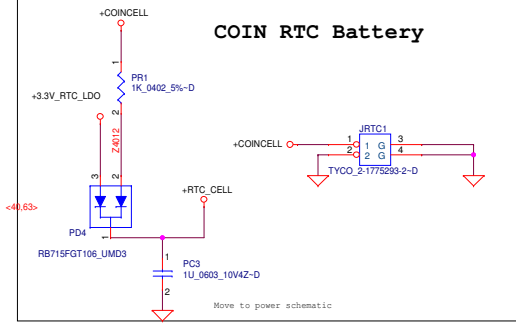
Media Bay Battery Connector



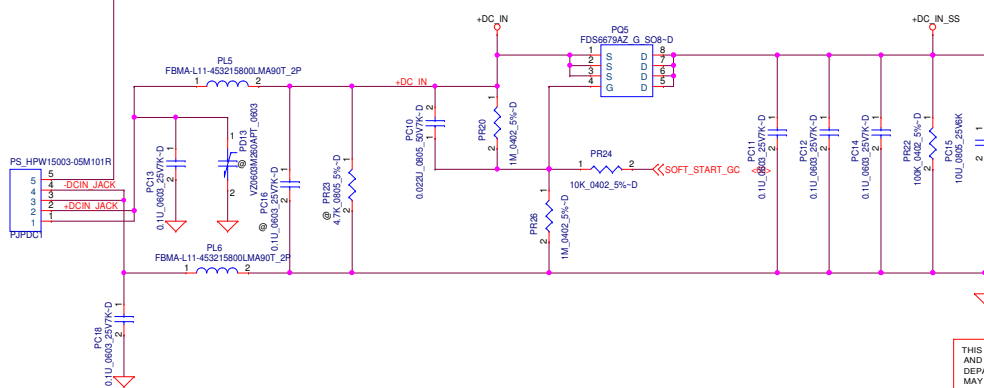
Primary Battery Connector



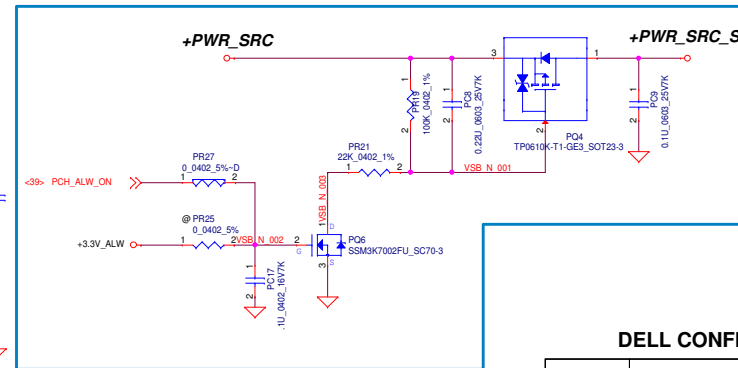
COIN RTC Battery




DC_IN+ Source



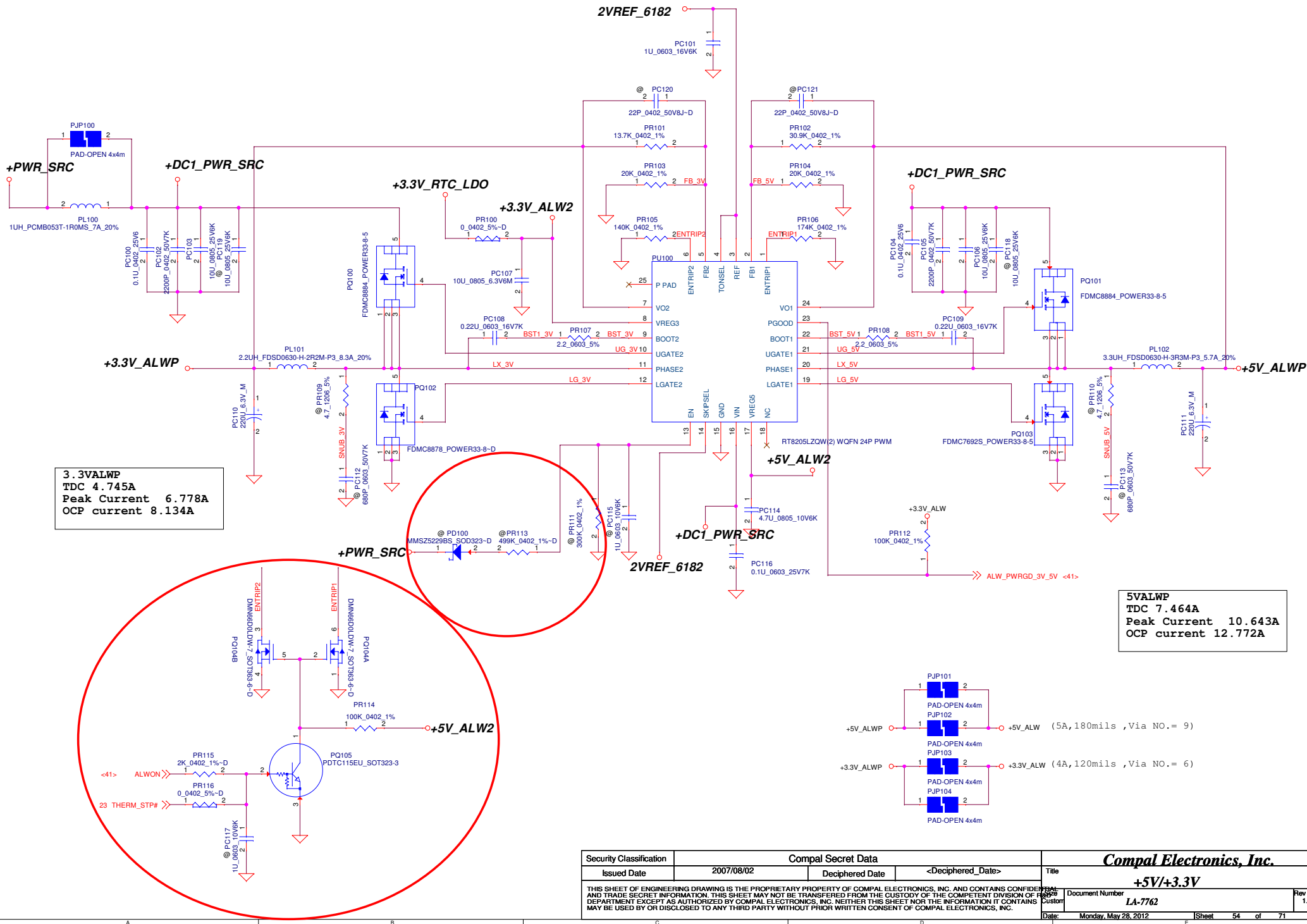
+PWR_SRC



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		+DCIN	
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+PWR_SRC

1.5Volt +/- 5%
TDC 12.248A
Peak Current 14.698A
OCP current 17.637A

+1.5V_MEN_P

Mode Level +0.75V_P +V_DDR_REF
S5 L off off
S3 L off on
S0 H on on
Note: S3 - sleep ; S5 - power off

+1.5V_MEN_P

+1.5V_MEM

+0.75V_P

+0.75V_DDR_VTT

(2A, 80mils , Via NO. = 4)

0.75Volt +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A

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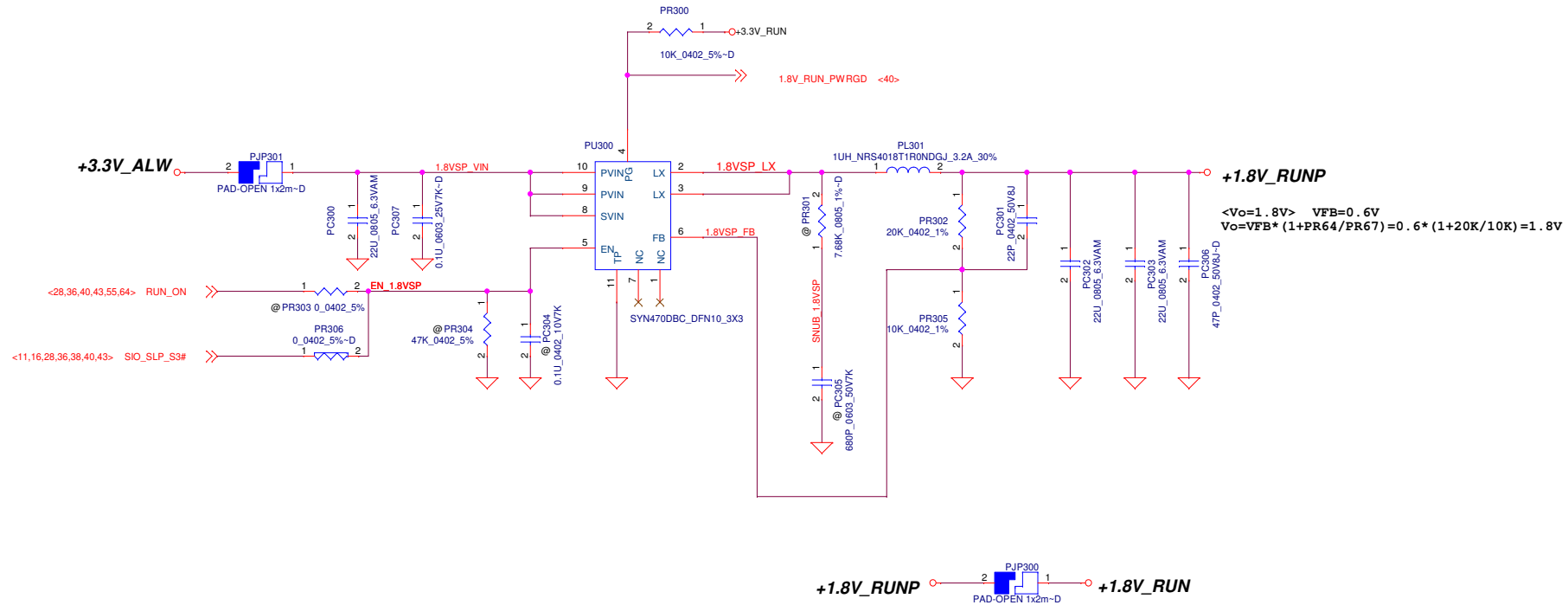
Compal Electronics, Inc.

+1.5V_MEN/+0.75V_DDR_VTT

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1.8Volt +/-5%
TDC 0.81A
Peak Current 1.157A
OCP current 1.388A



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+1.8V_RUN

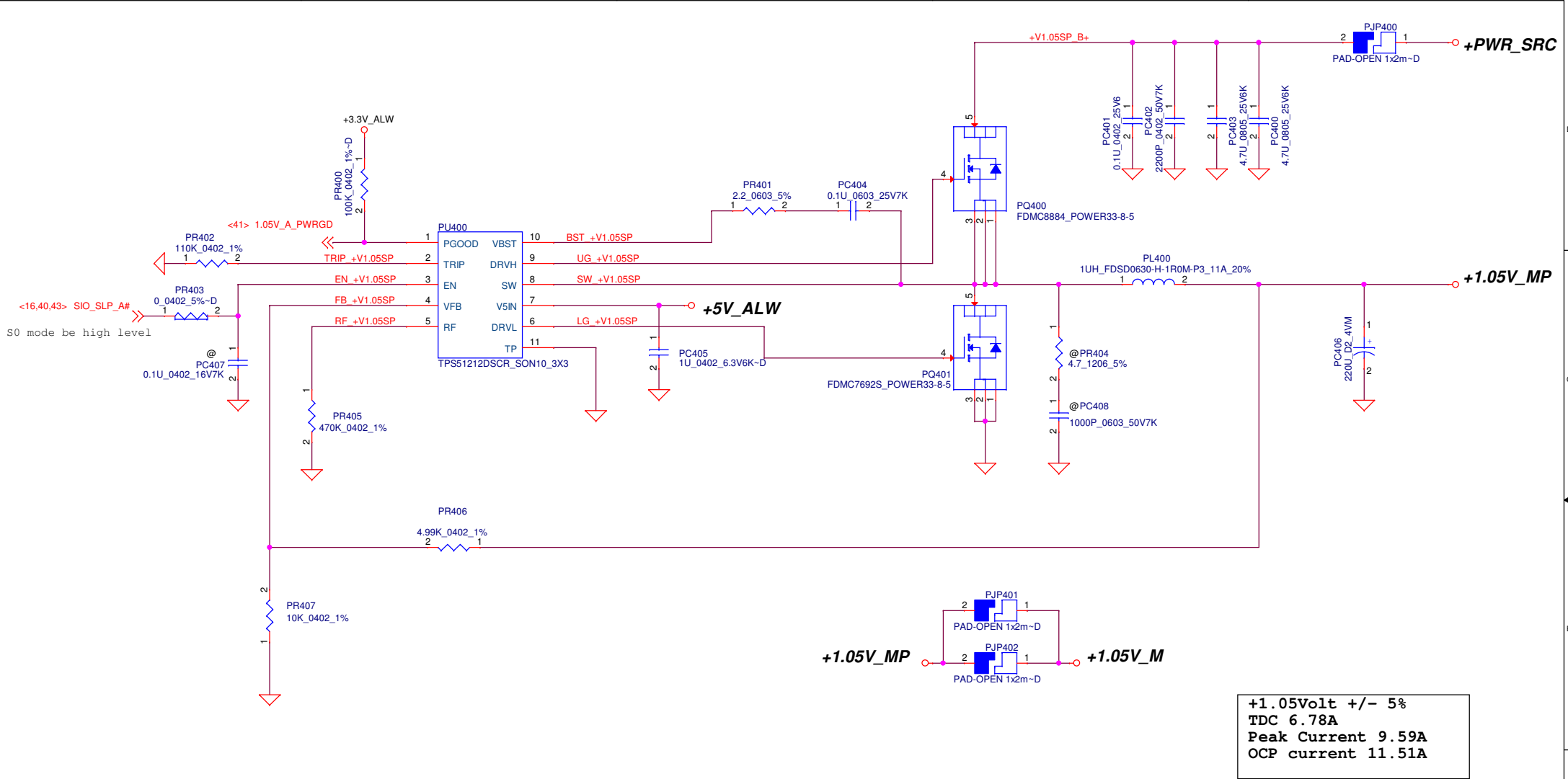
Document Number

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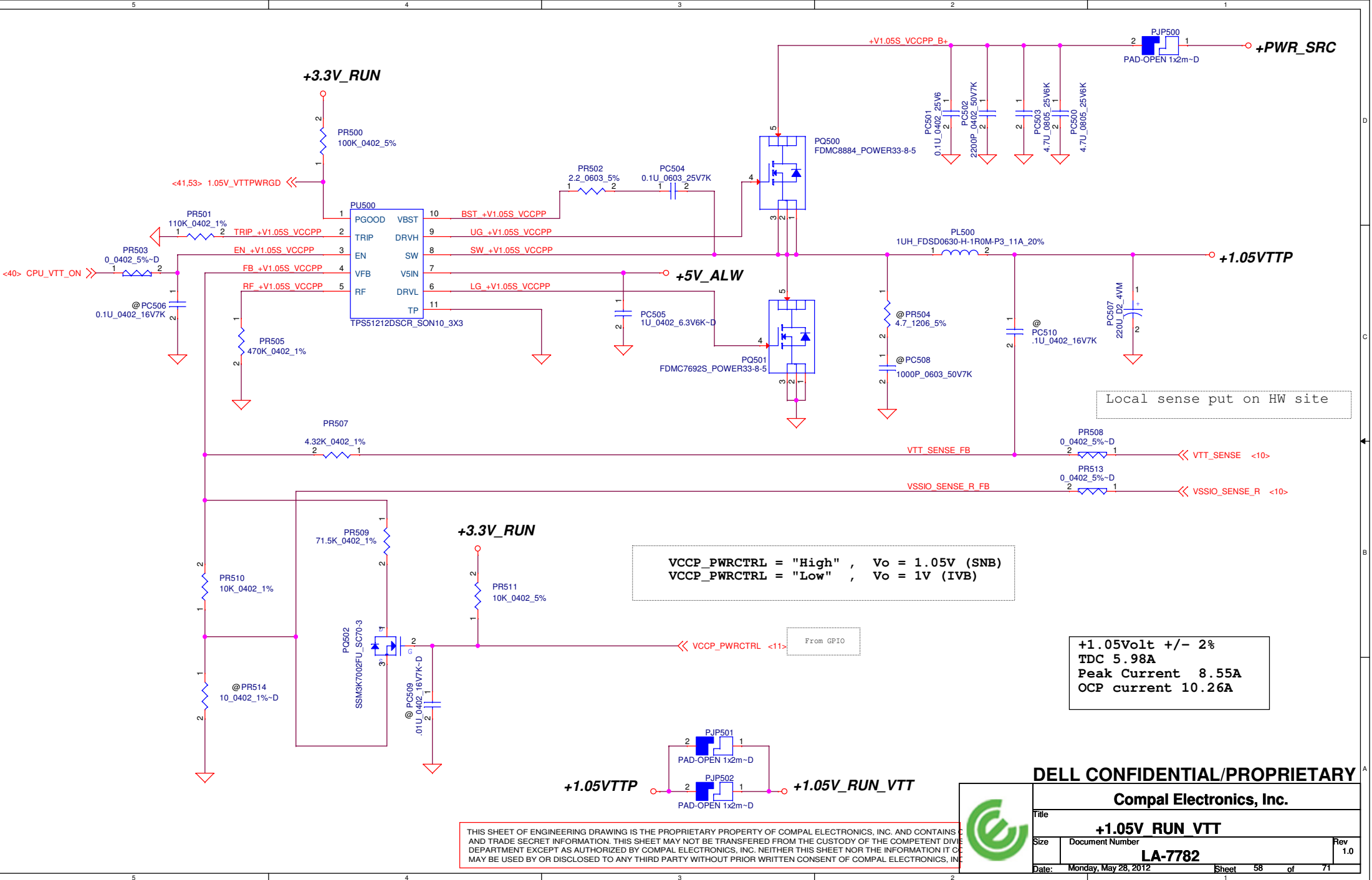
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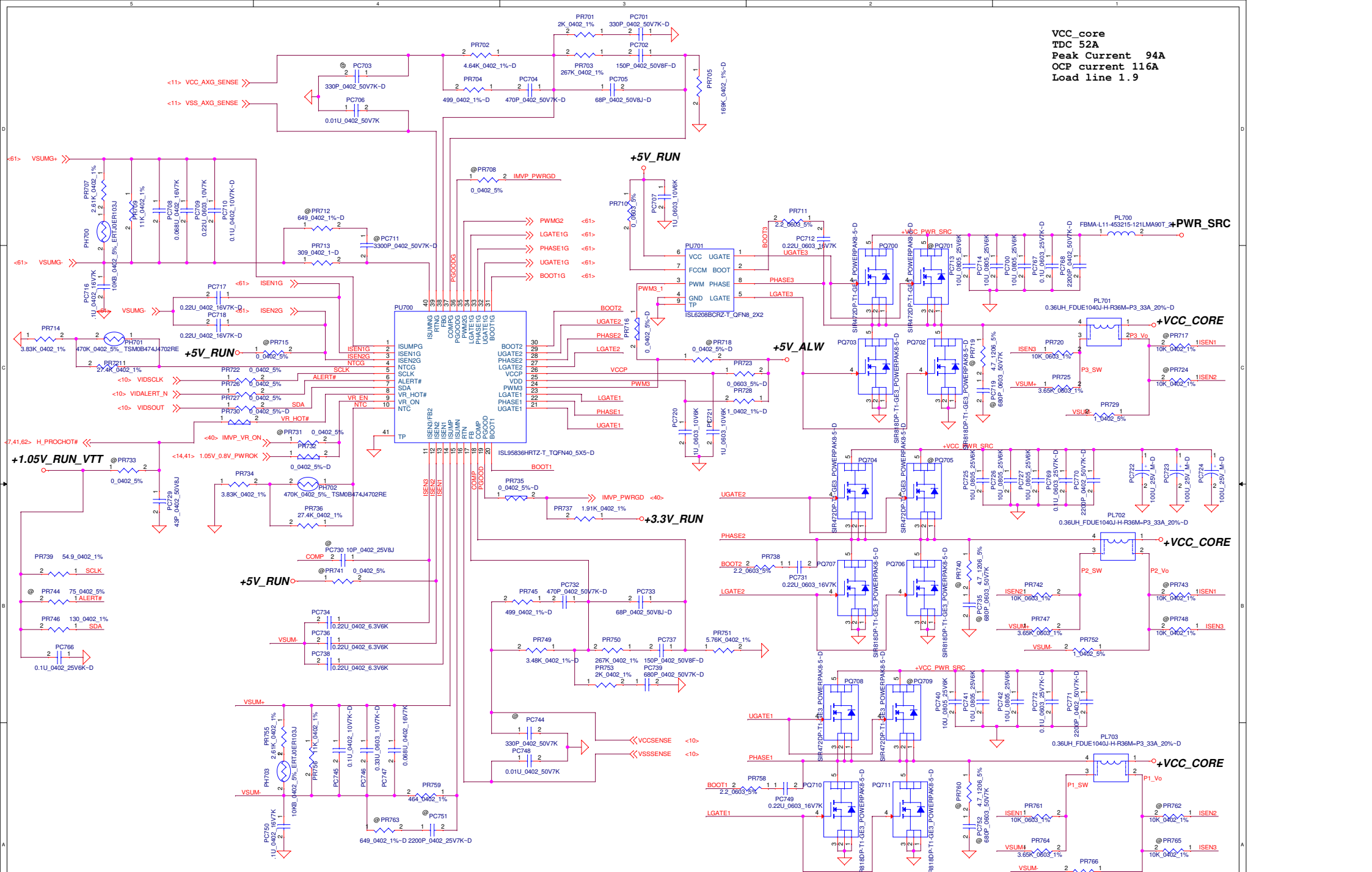
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+1.05V RUN VTT		
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VCC_core
TDC 52A
Peak Current 94A
OCP current 116A
Load line 1.9

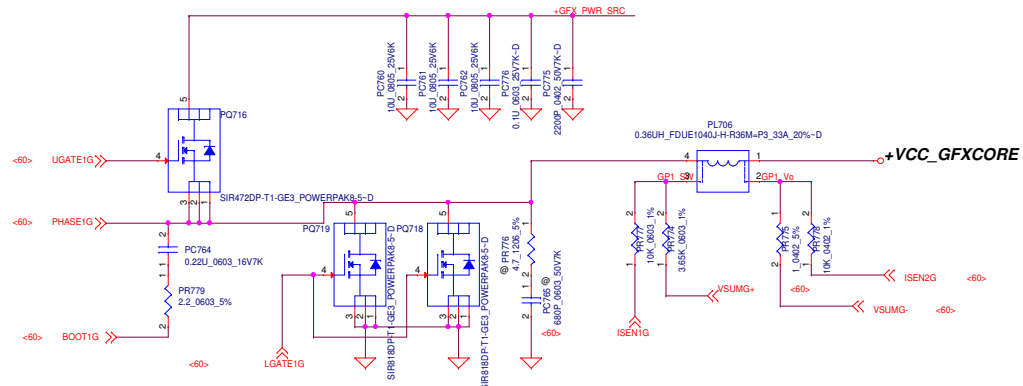
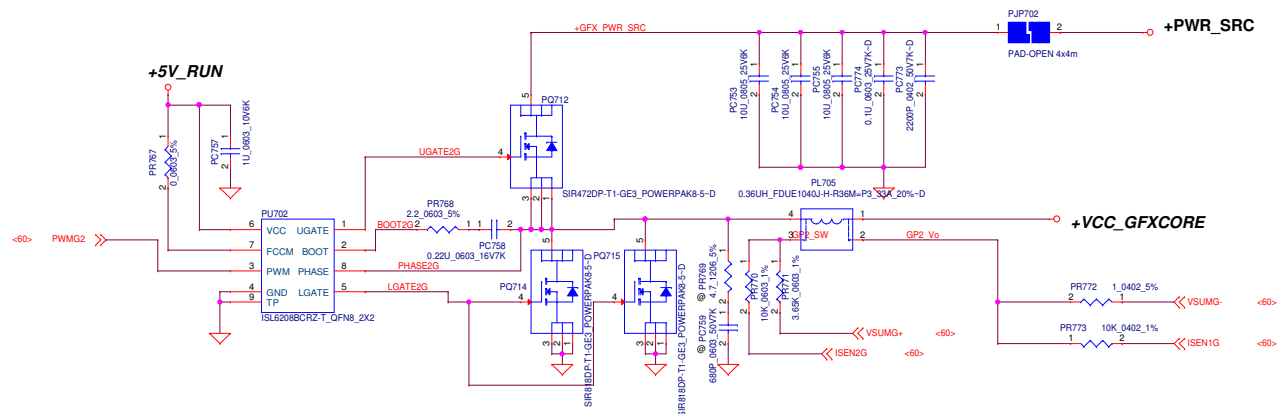
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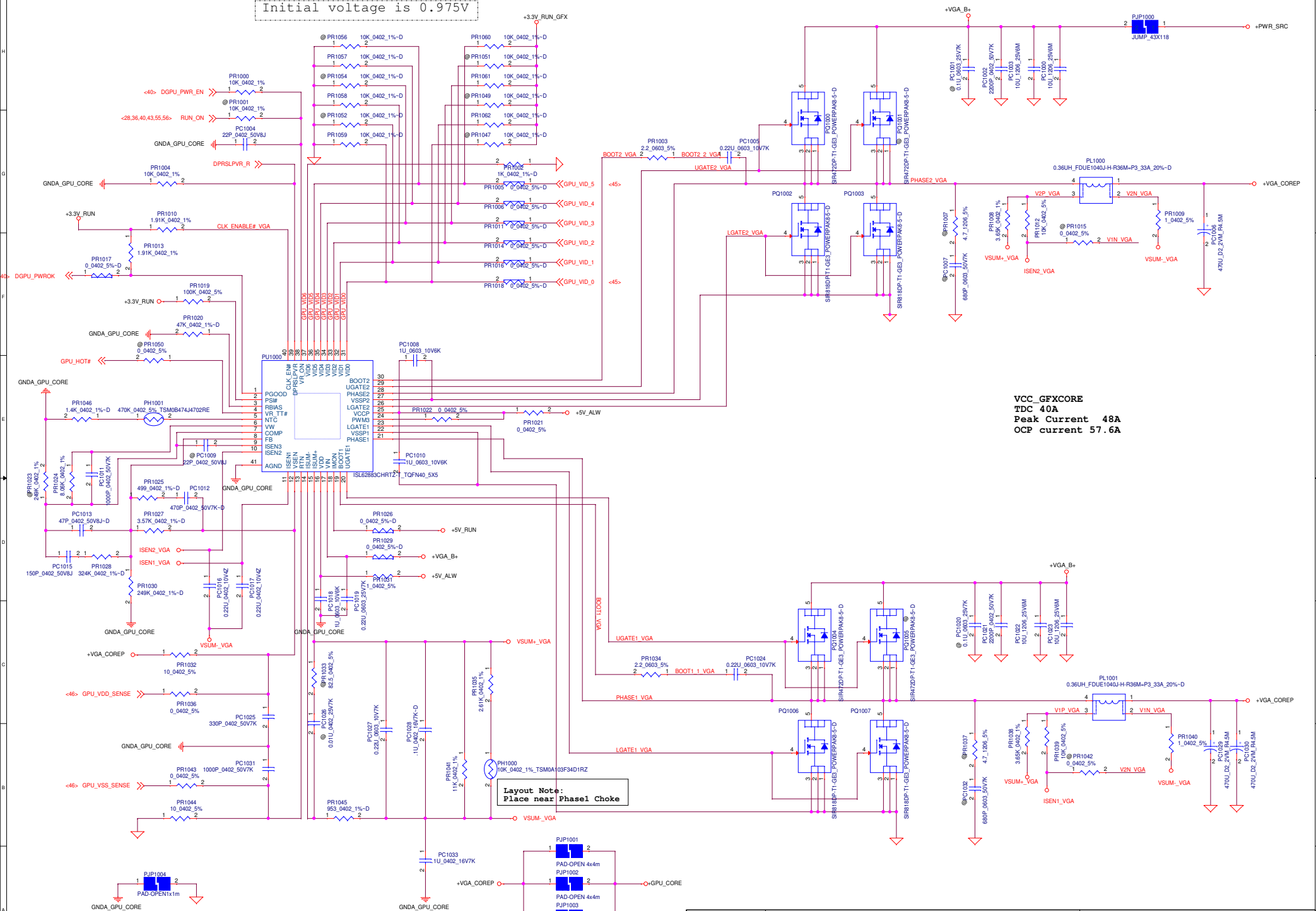


Compal Electronics, Inc.			
+VCC_CORE			
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```
VCC_GFXCORE
TDC 38A
Peak Current 46A
OCP current 57.18A
Load line 3.9
```



Initial voltage is 0.975V



VCC_GFXCORE
TDC 40A
Peak Current 48A
OCP current 57.6A

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	HW	6/21/2011	NV	NV strap setting update.	1. Stuff RV51,RV60,RV52,RV59. 2. Not Stuff RV53,RV54,RV57,RV97,RV99. 3. Change RV52 to 15K Ω . 4. RV53 with 45.3K 1% for Samsung 64Mx32; with 34.8K 1% for Hynix 64Mx32.	X01
2	37	HW	6/21/2011	COMPAL	USB3.0 & E-SATA behavior error.	U48 pin 10 & pin6 swap, and pin4 & pin5 swap.	X01
3	41	HW	6/21/2011	COMPAL	Modify Touch Pad circuit	De-pop R1162.	X01
4	11	HW	6/21/2011	INTEL	Follow INTEL check list Rev1.5.	RC99 ,RC100 change to 100 Ω	X01
5	31	HW	6/21/2011	IDT	IDT request.	PJP62 change to "JUMP_43X118".	X01
6	29	HW	6/21/2011	COMPAL	Modify WWAN circuit.	JMINI1 pin1 contact to PCIE_WAKE#.	X01
7	34	HW	6/21/2011	COMPAL	Follow E4 VC +3.3V_SUS Source circuit .	Reserve SIO_SLP_S4# contact to Q53 pin2.	X01
8	42	HW	6/27/2011	COMPAL	Leverage 14" schematic to modify Codec circuit.	Remove R167 & R178 (0 Ω) .	X01
9	30	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify PCH_GPIO16 pull-up resistor.	Change RH272 from 8.2K Ω to 10K Ω .	X01
10	18	HW	7/18/2011	COMPAL	Leverage 14" schematic to modify CAM_MIC_CBL_DET# pull-up resistor.	Change RH331 from 8.2K Ω to 10K Ω .	X01
11	43	HW	7/18/2011	COMPAL	Load SW sources output rising time mismatch and COS,cost concern.	Change back to E3 +3.3V/5V_RUN discrete solution	X01
12	15,45	HW	7/28/2011	COMPAL	bass on vender measure crystal EA by pass.	CH18,CH19 change to 6.8pF. CV34,CV35 change to 15pF.	X01
13	35	HW	7/28/2011	COMPAL	Follow INTEL check list(Rev1.5) change PCH GPIO52(PCIE_MCARD2_DET#) pull up resistor to 10K Ω .	Change R695 from 100K to 10Kohms.	X01
14	45	HW	7/28/2011	COMPAL	DGPU_PEF_RST abnormal during power on.	Change UV14 power to +3.3V_ALW.	X01
16	33	HW	7/28/2011	COMPAL	INTEL power sequence fail on T13(+1.8V_RUN to H_CPUPWRGD assert) due to USH move to sub-board but "USH_PWR_STATE#" no PU/PD for default.	Add R1640, 1M ohms pull down for USH_PWR_STATE# at M/B side	X01
17	11	HW	7/28/2011	COMPAL	Follow INTEL check list Rev1.5 for "VCCIO_SEL" , series resistor no stuff .	De-pop RC140	X01
18	41	HW	7/28/2011	COMPAL	Change board ID to X01	Change R875 to 130Kohms	X01
19	24	HW	7/28/2011	COMPAL	VCC tolerance of U3 is changed to 3.3V	Change U3 to SA00002VK00	X01
20	24	HW	7/28/2011	COMPAL	DELL requests PWM control flexibility.	Reserve D71 for PWM,but de-pop.	X01
21	20,43	HW	7/28/2011	COMPAL	Turn on +5V_ALW_PCH MOSFET Vgs less than cut-in voltage in battery mode.	Add control circuit for +5V_ALW_PCH	X01

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22	40	HW	7/28/2011	SMSC	SMSC no support function for LPC_LDRQ0#.	Delete net, LPC_LDRQ0#. Leave LDRQ0# no connection on both of 5048 and PCH side	X01
23	30	HW	7/28/2011	IDT	CODEC is change to 92HD93.	Pop R162~R166 and de-pop U73.	X01
24	30	HW	7/28/2011	IDT	Co-lay 92HD93 circuit for I2S BUS control.	Reserve 0 Q(R1641) to connect Codec Pin48 of the Codec and EN_I2S_NB_CODEC#.	X01
25	43	HW	8/3/2011	COMPAL	Modify +1.5V_RUN load switch circuit for POWER team suggestion.	Change Q59 from NTGS4141NT1G to AO4728L.	X01
26	16	HW	8/3/2011	COMPAL	Follow INTEL Power down sequence Tc timing fail(BITS:DF493966).	Add AND Gate(TC7SH08FU) input connect PM_APWROK & SIO_SLP_A# , and output connector PM_APWROK_R.	X01
27	42	HW	8/4/2011	COMPAL	Reset IC threshold voltage issue	Change U4 to RT9801A (threshold adjustable).	X01
28	17	HW	8/4/2011	COMPAL	Intel Review Feedback for PCH_GPIO3.	POP RH332.	X01
29	30	HW	8/4/2011	COMPAL	Co-lay 92HD93 with ALC290	Modify codec schematics	X01
30	14	HW	8/4/2011	COMPAL	SPI debug connector interfere power CAP(PC208) change connector type.	Change JSPI1 connector to SP01001DQ00.	X01
31	11	HW	8/5/2011	COMPAL	CH94 and CH95 to D2 size for cost concern	Change CH94 and CH95 from SGA0000170L to SGA00004L0L	X01
32	44	HW	8/11/2011	COMPAL	White light LED brightness is abnormal	change the resistor value: R934 change to 1K,R938 & R955 change to 1.8K,R939 change to 1.4K,R949 & R958 change to 620 and R957 change to 220.	X01
33	11	HW	8/12/2011	COMPAL	S3 resume issue.	Pop RC79 and de-pop RC82.	X01
34	37	HW	8/29/2011	COMPAL	USB3.0 Tx AC coupling follow CRBboard.	change C412 & C413 to 0.1uF.	X01
35	19	HW	8/29/2011	COMPAL	CRT ripple garbage display issue.	change LH1 to 1uH inductor,Change CH36 from 10uF(0603) to 22uF(0805).	X02
36	44	HW	8/29/2011	COMPAL	White light LED brightness is abnormal.	change the resistor value: R934 change to 1K,R938 & R955 change to 1.8K,R939 change to 1.4K,R949 & R958 change to 620 and R957 change to 220.	X02
37	30	HW	9/28/2011	IDT	Audio no sound issue in Dalmore 15 UMA. (BITS:DF504001).	Add C-R snubber circuit,C973~C976(2200P),R1658~R1661(3.3Ω).	X02
38	41	HW	9/28/2011	COMPAL	EC has internal pull up for volume signals.	De-pop R1169, R1197, R1118.	X02
39	43	HW	9/28/2011	COMPAL	+3.3V_RUN boot leakage issue.	Pop Q69 & R929.	X02
40	43	HW	9/29/2011	COMPAL	DMN3030LSS-13 poor soldering issue.	change Q55,Q61 to AO4478L.	X02
41	40	HW	9/29/2011	COMPAL	SMSC change ECE5048 Pin A23 to GPIO0.	Link ECE5048 symbol.	X02
42	41	HW	10/12/2011	SMSC	SMSC review feedback.	Reserve R1656 and R1657 100Kohms to GND for I2S disabled.	X02
43	43	HW	10/12/2011	COMPAL	+3.3/5V_RUN inrush current issue with 470pF.	Change C763 and C766 form 470pF to 220pF.	X02

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44	30	HW	10/12/2011	COMPAL	Remove ALC290 co-lay circuit.	Remove R1646, C1164, R1644, R1643, R1642, R171, C1204, C1205, R1647, C1165, R1648 and R1645.	X02
45	40	HW	10/13/2011	COMPAL	When suspend/resume cycles, wireless SW GPIO IRQs keeps giving	Add R771 pulling up to +3.3V_ALW for WIRELESS_ON#/OFF and de-pop R766.	X02
46	42	HW	10/13/2011	COMPAL	Chane reset IC to RT9818A-44GU3.	Update U4 symbol and add R1629 for backup of inrush prevention. Change RSMRST# pull up with 100Kohms. Pop R1655 and de-pop R1623.	X02
47	42	HW	10/13/2011	COMPAL	Change board ID to X02.	Change R875 to 62Kohms.	X02
48	34	HW	10/13/2011	COMPAL	EMI request to change SD CLK series R.	R676 is changed from 33ohms to 10ohms.	X02
49	ALL	HW	10/13/2011	COMPAL	For cost saving.	Change 0 ohm resistor to short pad.	X02
50	44	HW	10/13/2011	COMPAL	DFX request to change CILP PAD.	Change CLP1 PAD from "79X138" to "110X138" .	X02
51	22	HW	10/21/2011	COMPAL	VSET Setting change Tp from 88 degree to 93 degree.	change R406 from 953Ω to 1.33KΩ.	X02
52	17, 35.	HW	11/08/2011	COMPAL	PCH GPIO52 changed to be free.	De-pop R725, remove R695 and add RH359.	X02
53	ALL	HW	11/08/2011	COMPAL	For cost saving.	Change 1Kohms +-1% to +-5% except RC78, RC80, RC81, RC84, RV32, RV45, RV47 and RV48.	X02
54	11, 43	HW	11/14/2011	COMPAL	AO4728L leakage issue.	Change QC3 and Q59 to AO4304L (SB00000RV00) .	X02
55	33	HW	11/14/2011	COMPAL	+3.3V_RUN Giltch when AC plugin.	Add D87, R1666 and R1665 for HW solution backup.	X02
56	45	HW	11/15/2011	COMPAL	pop option for GPU deeper sleep mode.	Add net name, DPRSLPVR on GPU GPIO16 and reserve RV131.	X02
57	14~21	HW	11/16/2011	COMPAL	Change PCH to C0 version.	Change UH4 to SA00005BU0L.	X02
58	39	HW	11/16/2011	COMPAL	EMI request to add 33Ω for DP port.	Add 33ohm on DPD_DOCK_LANE_P0/N0, DPD_DOCK_LANE_P1/N1, DPD_DOCK_LANE_P2/N2, DPD_DOCK_LANE_P3/N3, DPC_DOCK_LANE_P0/N0, PC_DOCK_LANE_P1/N1, DPC_DOCK_LANE_P2/N2, PC_DOCK_LANE_P3/N3.	X02
59	11, 24, 29, 43, 49.	HW	11/16/2011	COMPAL	Change RC value at Gate of MOS Load SW to modify power rail soft start timing.	RC72 from 100K to 330K; RC143 form 330K to 1M; CC136 form 0.1u to 0.022u R412 from 100K to 470K; R1632 form 1M to 4.7M; C293 form 0.1u to 0.022u R507 from 100K to 470K; R517 form 1M to 4.7M; C400 form 0.1u to 0.022u R722 from 100K to 470K; R1625 form 1M to 4.7M; C644 form 4700p to 220p R729 from 100K to 470K; R1628 form 1M to 4.7M; C650 form 4700p to 220p R917 from 100K to 470K; R1617 form 1M to 4.7M; C770 form 4700p to 220p R920 from 100K to 470K; R1610 form 470K to 2.2M; C771 form 4700p to 470p R930 from 330K to 470K; R1611 form 470K to 1M; C773 form 2200p to 100p R906 from 100K to 470K; C763 form 2200p to 220p R912 from 100K to 470K; C766 form 470p to 220p RV73 from 100K to 470K; RV81 form 470K to 2.2M; CV132 form 2200p to 100p RV67 from 100K to 470K; RV80 form 470K to 2.2M; CV129 form 2200p to 100p RV91 from 100K to 470K; RV94 form 1M to 4.7M; CV186 form 3300p to 220p	X02
60	26	HW	11/29/2011	COMPAL	EMI final solution for HDMI.	1. L19/L20/L21/L22 de-populated & R459/R451/R462/R466/R468/R469/R470/R471 populated 0 ohm. 2. Change R467 from 499ohms to 510ohms to adjust sigal swing. 3. Pop R486 & R487 to enable HDMI repeater pre-emphasis. De-pop LC filter at HDMI conn. side.	X02
61	17, 35, 39.	HW	12/05/2011	COMPAL	EMI solution for E-Docking USB port.	Swap USB Port6 and Port8 and reserve a choke at E-Docking conn. side: Port6 from Mini3 Pink Panther card to E-docking Port8 from E-Docking to Mini3 Pink Panther card	X02
62	36	HW	12/05/2011	COMPAL	From ESD team request	Add 0.1u CAP for EXP PWR SW signals, CPUSB#, EXPRCRD_CPPE# and CARD_RESET#	X02

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63	40,45	HW	12/05/2011	COMPAL	Power over rating when using 65W adapter	Add EC5048 GPIOA7, GPU_PWR_LEVEL to slow down GPU when GPU keeps at high performance mode but using 65W adapter	X02
64	14~21	HW	12/05/2011	COMPAL	Change PCH to C1 (QS) version.	Change UH4 to SA00005BU1L.	X02
65	32	HW	12/06/2011	COMPAL	EMI request for ISN Issue.	Add ESD diode on GND_CHASSIS trace if EMI change C485:1000P to 120P.	X02
66	7	HW	12/06/2011	COMPAL	ESD Request.	RC19.2 change to XDP_DBRESET#_R. RC29.2 change to XDP_TDI_R. RC35.2 change to XDP_TDO_R.	X02
67	24	HW	12/06/2011	COMPAL	EMI request for USBP12.[BITS:DF524330]	Pop L12 and De-pop R427,R428.	X02
68	41	HW	02/01/2012	COMPAL	Change board ID to A00.	Change R875 to 33Kohms.	A00
69	32	HW	02/01/2012	COMPAL	30MHZ~50MHZ LAN broadband noise.	Modify C485 from 10pF to 150pF.	A00
70	44	HW	02/20/2012	COMPAL	ME Request.	SW1 change to SN11100580L.	A00
71	All	HW	02/20/2012	COMPAL	For cost saving.	Change 0 ohm resistor to short pad, total 14 pcs.	A00
72	28	HW	02/20/2012	COMPAL	For cost saving.	HDD PWR De-pop :R1624, R500, R499, R504,R516,Q28, C393, C394.	A00
73	14	HW	02/20/2012	COMPAL	For cost saving.	De-pop RH288,RH48,RH49,RH47.	A00
74	7	HW	02/20/2012	COMPAL	ESD Request.	De-pop RC30, RC31, RC33, RC34, RC36, RC37, RC38, RC39 .	A00
75	37	HW	02/20/2012	COMPAL	System will reconnect USB 3.0 after resume from S3 issue.[BITS:DF537410].	JBTB1 Pin 38 reserve R154 to +3.3V_ALW_PCH.	A00
76	35	HW	02/20/2012	COMPAL	E4 no support WWAN SMBUS function .	Not stuff R1157 and R1158.	A00
77	36	HW	02/21/2012	COMPAL	Fix EMI issue.	Stuff CE16,CE17 & CE18.	A00
78	37	HW	02/21/2012	COMPAL	Dell E4 NB USB1457 Samsung i9100 S0 issue	Add Q126 and remove R1613.	A00

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1	55	+1.5V_MEN	7/5	Dell	Follow VC , enable use SIO_SLP_S4#.	Add PR210 for net "SIO_SLP_S4#"	X01
2	53	DCIN	8/4	Dell	ME design change.	PJPDC1 change from 7pin to 5pin	X01
3	54	+5V/3.3V	8/4	Dell	Main and 2nd IC common setting.	De-pop PD100,PR113,PR111	X01
4	60,62 54	Vcore, Charger +5V/3.3V	8/4	Compal	EMI solution.	Pop PL700.PL1300,PL100	X01
5	54	+5V/3.3V	8/4	Compal	DFX concern, choke change from 10*10 to 7*7	PL101 change from 3.3u 10*10 to 2.2u 7*7 PL102 change from 3.3u 10*10 to 3.3u 7*7	X01
6	54 55	+5V/3.3V +1.5V_MEN	8/4	Compal	COS concern, change from D2 Polymer cap to OScon cap	PC110 change from 220u polymer cap to 220u OScon cap PC208 change from 330u polymer cap to 390u OScon cap	X01
7	54 55	+5V/3.3V +1.5V_MEN	8/4	Compal	Prevent Jitter issue.	Add PC120,PC121,PC215 parallel with PR101,PR102,PR207	X01
8	60	Vcore/GFX core	8/4	Compal	Prevent output voltage glitch when power up.	PU700, VCCP and VDD change form +5V_RUN to +5V_ALW	X01
9	64	GPUcore	8/4	Compal	Prevent output voltage glitch when power up.	PU1000 VCCP and VDD change form +5V_RUN to +5V_ALW	X01
10	60	Vcore/GFX core	8/4	Compal	DFX concern.	Change PU701,PU702 from ISL6208(3x3) to ISL6208B(2x2).	X01
11	60	Vcore/GFX core	8/4	Compal	Fine tune the VCORE and VGFX Load Line	Change PR749 from 3.57K to 3.48K Change PR702 from 3.57K to 4.64K	X01
12	60	Vcore/GFX core	8/4	Compal	Fine tune the VCORE and VGFX transient response	Change PC733 &PC705 from 47pF to 68pF Add PC708 0.022uF	X01
13	62	Charger	8/4	Compal	Change the component to HF parts	Change PQ1306 & PQ1308 from SB50206008L to SB57002040L	X01
14	53	DCIN	10/17	Compal	Reduce power consumption in S5.	Add PCH_ALW_ON for +PWR_SRC_S enable signal.	X02
15	64	GPUcore	10/17	nVidia	Deep sleep mode control.	Add DPRSLPVR_R signal connect to GPU.	X02
16	60	Vcore/GFX core	10/17	Compal	Fine tune the VCORE transient response	Add PC747 68nF	X02

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1	54-64		10/20	Compal	For cost saving, change the 0ohm resistors to layout short PAD.	Footprint change PR100,PR116,PR208,0R210, PR306,PR403,PR503,PR508,PR513,PR600,PR602, PR604,PR607,PR612,PR716,PR730,PR732,PR735, PR1300,PR1302,PR1312,PR1320,PR1339,PR1342, PR911,PR925,PR937,PR941,PR932,PR936,PR926, PR935,PR945,PR947,PR949,PR939,PR940,PR943, PR948,PR951,PR955,PR957,PR961,PR953,PR954, PR956,PR958,PR959,PR960,PR963,PR1005,PR1006, PR1011,PR1014,PR1016,PR1018,PR1017,PR1026, PR1029	X02
2	55	+1.5V_SUS	10/20	Compal	Fine tune OCP.	PR201 change form 5.1K to 6.34K.	X02
3	57	+1.05VM	10/20	Compal	Fine tune OCP.	PR402 change form 60.4K to 110K.	X02
4	58	+1.05VTT	10/20	Compal	Fine tune OCP.	PR501 change form 84.5K to 110K.	X02
5	60	Vcore/GFX core	02/15	Compal	Fine tune the VGFX transient response for 3rd source choke	Change the PC708 from 22nF to 68nF	X03

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